An investigation into effective cooling techniques for micro-electric systems

Shirvani, Hassan

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AN INVESTIGATION INTO EFFECTIVE COOLING TECHNIQUES FOR MICRO-ELECTRONIC SYSTEMS

Submitted by

Hassan Shirvani

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School Of Mechanical Engineering,

University Of Bath

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To my father, mother and wife
Buick, Afsar, and Catherine

Hassan Shirvani

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NOTATION

A	surface area	m^2
A_c	cross-sectional area	m^2
D	diameter	m
D_e	equivalent diameter	m
f	friction factor	
F	shape factor	
h	heat transfer coefficient	W/m^2C
K	thermal conductivity	W/mC
L	characteristic length	m
J^R A	junction-to-ambient thermal resistance	°C/W
J^R C	junction to case thermal resistance	°C/W
C^R A	case to ambient thermal resistance	°C/W
P	pressure	N/m^2
ΔP	pressure drop	N/m^2
Q	heat transfer rate	W
q_i	internal energy generation	W/m^3
s	PCB mounting pitch	m
T	temperature	°C
T_A	ambient temperature	°C
T_S	surface temperature	°C
T_J	junction temperature	°C
T_{bulk}	mean mix temperature of the fluid	°C
T_{ad}	adiabatic temperature	°C
Z	influence coefficient	°C
V	velocity	m/s
v	volume	m^3
μ	dynamic viscosity	Ns/m^2
υ	kinematic viscosity	m^2/s
C_p	heat capacity	J/kgC
θ	temperature difference	°C
σ	Stefan-Boltzmann constant	W/m^2K^4
ε	emmisivity	
ρ	density	kg/m^3

DIMENSIONLESS GROUPS

Re	Reynolds number	VL/υ
Pr	Prandtl number	$\mu C_p/K$
Gr	Grashof number	$\beta g\rho^2L^3\theta/\mu^2$
Nu	Nusselt number	hl/K
Bi	Biot number	hL/K

SYMBOLS IN THE FINITE ELEMENT FORMULATION

[K]	element matrix
N_i	trial functions or shape functions
u_i	degrees of freedom (DOF).
u()	dependent field variable
c_0 to c_4	constants
x,y,z	independent variables
M	number of independent functions
f(x)	function
R(x)	residual
u	vector of nodal displacements
p'	load vector

ABBREVIATIONS USED

IR	infra-red
DIPs	dual-in-line packages
SMCs	surface-mounted components
PCB	printed circuit board

SUMMARY

This thesis presents an accurate experimental and theoretical study of the complex three dimensional heat transfer involved in a microelectronic system. Accurate thermal analyses of the miniature electronic packages were achieved by developing new experimental techniques, and the construction of realistic three dimensional finite element models.

The assessment of the various methods of temperature measurement for electronic packages mounted on a printed circuit board, led to the design and development of a non-contact infra-red scanning device. This was incorporated into a forced convection heat transfer research rig. In a comprehensive experimental investigation, data were obtained for a range of airspeed and power dissipations. It was demonstrated that the temperature levels of the downstream modules were largely influenced by the heated wakes shed by the powered modules upstream. The principle of superposition was used to sum these effects to predict module temperatures for the case when the modules are not uniformly powered.

Because the silicon chip itself is encapsulated, it was necessary to develop a novel electronic method to measure its temperature. An on-board temperature sensitive component (the substrate isolation diode) was used as a resistance thermometer. To measure chip temperatures at normal load a high speed electronic switching circuit was designed and built. This method of measuring peak junction temperatures, complemented the external surface temperatures from the IR scanner. Using this method accurate transient thermal analysis of chiprack and DIPs was carried out.

The theoretical work has largely been concentrated on using the finite element method to build detailed, realistic thermal models of the electronic systems. Experience has shown large amount of data produced by these models, validated and complemented by the experimental data from IR scanner, form a powerful method of thermal analysis, particularly for these miniature, inaccessible devices.

The state of the art electronic packages (surface mount components) were also investigated, In a series of experiments and finite element runs the unknown thermal conductivity of the plastic encapsulant was deduced. The present work also provides a correlation for heat transfer coefficient over an array of uniformly powered SMCs mounted on a custom made printed circuit board.

CHAPTER 1

INTRODUCTION

1.1 THE PROBLEM IDENTIFICATION

All semiconductor devices consume an appreciable amount of electrical energy and converts it to heat. Heat transfer engineering is playing an increasingly important role in the advancement of electronic technology.

Concerns over the short life of vacuum tubes due to over heating seemed to end with the invention of the transistor in December 1947 [1]. It was considered that this invention, because of their relatively low power requirements, would greatly reduce, if not totally eliminate, all cooling concerns. Such hopes, however, were short lived, as engineers sought to improve performance, cost, and reliability by packaging greater numbers of circuits in an ever smaller space. In fact circuit densities have increased dramatically over the years Figure 1.1. For instance in an electronic system a 5x5 mm chip dissipating 10W is not unheard of, and this results in a heat flux of 4×10^5 W/m^2. As shown in Figure 1.2a and Figure 1.2b, this is about two orders of magnitude less than that on the surface of the sun [2]. But the sun surface temperature is 6000° C, compared to a maximum operating temperature in the range of 100° C for a typical semiconductor chip.

The task of accommodating such high fluxes while maintaining relatively low component temperature, is the principal challenge faced by today's thermal engineers.

The acceptable operational temperature of electronic components are dictated not only by performance requirements, but also by increasingly stringent reliability demands. Because failure rate increases by a factor of about two for every 10 C increase in operating temperature [2] (near exponential dependence Figure 1.3), a downwards trend of both the mean component operating temperature, and the variation of the temperatures about the mean must be maintained if reliability is to be continuously improved. Thermal problems are further complicated by the fact that microelectronic devices need to operate in a wide range of environmental temperature. In practice the cooling scheme should be the most cost effective design choice which satisfies all or most of the performance criteria.

1.2 HEAT IN ELECTRONIC EQUIPMENT

The thermal management of a complex system made up of electronic components or sub-systems (e.g computer CPU boards) may be analyzed by carefully dividing the entire system into different structural levels. The structure of a typical system is illustrated in Figure 1.4, the chip, the module or package, the printed wiring board (PWB) or printed circuit board (PCB) and the system. The chip is a square or rectangular slice of single crystal silicon. A microscopic pattern of electronic circuits are impregnated onto the surface of the silicon through a number of chemical, thermal, mass transfer, optical and mechanical processes. The chip is isolated by enclosing it within an encapsulant or package, whose primary function is to protect the chip from the atmosphere. The electrical leads which transmit the pulsed signals into and out of the package are also housed within the package. The body of the package may in

some cases, depending on its thermal properties, present a significant thermal resistance to heat removal from the chip embedded within it. In some cases where the package possesses a large power dissipation, a finned heat sink device maybe mounted on the surface of the package to enhance heat transfer to the coolant. A package may contain more than one chip, in which case the package is referred to as module. Packages and modules are mounted on the printed circuit board (PCB) upon which a layer, or layers, of copper tracks are fabricated. The PCBs are mutually connect by wiring or other means to the power supply. A fan may be mounted within the system for coolant enhancement to transport the energy to the ultimate heat sink.

The goal of sound thermal design, in conditions of ever increasing circuit density, is to find a solution which meets the requirements set by the electronic performance. Heat produced by the chip travels along multiple conduction paths within the package, overcoming the internal thermal resistance . This resistance is a complex function of the geometric structure of the package or module, and the different materials of which it is constituted. Heat is transferred by convection from the external surface of the package to the coolant, overcoming the external resistance of the module. Techniques of heat transfer enhancement are beginning to play an important role on coping with the increased rates of heat dissipation from miniaturised packages.

At the overall system level the temperature of the coolant increases as the coolant cumulatively absorbs heat from the modules along its flow path. Packages near the exit of the coolant path are therefore subject to the most severe thermal environment due to high temperature of coolant surrounding them. Where air is used as coolant

the mass flow rate must be kept sufficiently high to maintain a reasonable air temperature at exit from the cooling channel [3].

1.3 HISTORY OF THE PROBLEM

For the past sixty five years the thermal management and control of electronic components has been one of the important areas of application of advanced heat transfer techniques. This has in turn led to improved reliability, while allowing increased power capability, higher frequency of operation and physical miniaturisation. In 1925 determination of the temperature distribution in the laminated core of a transformer by Cockcroft [4] constituted a pioneering attempt to apply heat transfer techniques to electronic component cooling. Ten years later Cockroft's work was followed by several key papers by Black and Sinnadurai [5, 6] applying air and liquid cooling to high power vacuum tubes. Marston [7] carried out a classic study of the design and optimization of a natural convection cooling of fine array of semiconductor packages.

Following World War II the rapid demand for use of electronic equipment in both the military and civilian sectors led to widespread recognition of the need for thermal packaging and design of complex electronic components and to the initiation of thermal management and control technology.

Despite the invention of the transistor in 1947, with its inherently lower power requirements, electronic systems continued to pose thermal problems. This was largely a consequence of the second revolution in manufacture and the invention of integrated

circuit. The trend to increased miniaturisation of individual circuits led to large scale integration (LSI) and very large scale integrations (VLSI). The incorporation of more and more miniature components in a chip allows the functionality of the chip to be continuously increased. Also, increased packing density allows signal transit time to be reduced. Increased clock speed and higher switching power, can also be used to give increased performance. Thus even though the power of an individual circuit may fall, the total power dissipation per chip has tended to increase.

During 1960's and 1970's novel cooling techniques such as immersion cooling, flow boiling, thermoelectric devices, etc. were developed. However, because of its inherent simplicity and low cost, air cooling, either natural or forced convection, continues to be the most commonly used mode of cooling.

1.4 PACKAGING TRENDS

i) DUAL-IN-LINE PACKAGES

A wide range of standard Integrated Circuits (ICs) are now available commercially, Figure 1.5. The dual-in-line package was the first widely used electronic package. General construction of such a device is illustrated in Figure 1.6a. The ends of the curved leads from the active layer normally pass through the mating holes on the PCB and are soldered to the copper tracking on the under side of the board for transmission of signals Figure 1.6b . These leads provide the path for heat conduction to the printed circuit board during operation Figure 1.8. In other cases these leads may be inserted into a socket that is itself soldered to the PCB. A plastic or ceramic is used to encapsulate the silicon die (with its integrated circuits) to protect the die from the

surrounding environment. This encapsulant constitutes resistance to conduction of heat from the die. The die may be mounted on a conducting flag connected to a tie-bar which enhances the conduction process from the junction to the external surface of the package. DIPs on a PCB with plated through hole (PTHs) constitute as much as 85% of the total manufactured electronic assemblies.

Although DIPs are still widely used in electronic industries, the limitation of these devices are due to their overall size and weight in comparison to the semiconductor die itself. Because of their geometric arrangement, and the manner of attachment to the PCB, DIPs become increasingly unattractive as the number of electrical connections (pin count) is increased. DIP packages with more than 64 pins are currently regarded as impractical because of surface area required on the PCB [8]. The principle advantage of DIPs are due to mechanical support provided by the flexible leads, which reduces the problem of thermal stress.

ii) SURFACE MOUNTED DEVICES

The disadvantages of DIPs have been overcome by the introduction of Surface Mounted Components (SMC) [8] Figure 1.8a. As the name suggests, these packages are mounted directly on the surface of the printed circuit board by means of a solder-foot print thus avoiding holes in the PCB and offering optimum surface efficiency. Because they have leads on all four sides of the package, surface mounted component can be much smaller than those typically used through-hole mounting, Figure 1.8b. A general internal and external construction of SMC devices is illustrated in Figures 1.9a and 1.9b. The result of such packaging is a higher packing density. Up to four times as many components can be mounted on a board, and more if components are

mounted on both sides of the printed circuit board. A size comparison of Dual-In-Line packages and SMCs is shown in Figure 1.10 . Other benefits include lower parasitic capacitances and inductances, higher reliability, fewer assembly related faults, reduced production costs and simplified handling of components.

The SMC devices, to some extent, poses more heat conduction path to the printed circuit board, because they have leads to all four sides of the package.

iii) THE CHIP CARRIER

The chip carrier was originally developed for the US military. It can be visualised as the centre portion of a DIP or SMC with the two rows of metal leads replaced by contact pads on all four sides. Figure 1.11a illustrates an EPIC chip carrier construction. Chip carriers can be leadless, leaded ceramic or plastic, and are attached to the printed circuit board via solder pads. Advantages of these devices include their smaller size, input/output contacts on four sides ensuring short contacts to the internal chip-cavity bond pads, and the consequent reduced parasitic resistance. Other advantages include space saving, as in case of surface mounted components as these can be mounted on both sides of the printed circuit boards. Figure 1.11b, represents the comparison of a typical chip carrier, and a Dual-In-Line package.

A type of a chip carrier which has recently been developed by Dowty Electronic is known as CHIP RACK. The chip is mounted in the centre of a miniature PCB with pad connections to all sides. The intention is to mount several of these carriers one above another to form a stacked system Figure 1.12 (This system will be dealt with in greater detail later).

1.5 STANDARD COOLING DESIGNS

When the heat has been conducted from the chip (heat source) to the surface of the component and PCB, it must then be transferred to the surrounding cooling medium by one of the following mechanisms:-

a) Radiation and natural convection.
b) Forced air cooling.
c) Forced liquid cooling.
d) Boiling.

The above list of heat transfer methods is arranged in order of increasing heat transfer effectiveness and of increasing system complexity. For a given package and PCB area, the least heat can be transferred by radiation and natural convection, and most can be transferred by boiling. Heat transfer by radiation and natural convection requires no auxiliary equipment. Forced air cooling requires a fan and fan controls. Forced liquid cooling requires a pump, coolant reservoir and cooling fluid. A notable example of advanced cooling design is the IBM thermal conduction module for their mainframe computers. In this module spring loaded aluminum pistons in a helium atmosphere, conduct the heat released by each chip to the aluminum piston and then to a water-cooled cold plate Figure 1.13a. Other examples of standard cooling are shown in Figure's 1.13b to 1.13d.

1.6 THERMAL MISMATCH

Variations in temperature can cause stresses at those interfaces where material of dissimilar temperature coefficient of expansion (TCOE), or dissimilar power dissipation, are in intimate contact. When sufficiently intense, these stresses will result

in catastrophic failure of semiconductor devices. One such situation can arise when plastic encapsulate is transfer moulded directly around a chip die and its bond wires. Since plastic possesses a much higher temperature coefficient of expansion than the wire, this will give rise to excessive strain, which can damage the wire. Normally such problems are largely overcome by deliberately loading the plastic with organic fillers so that a near match between its TCOE and that of the other materials inside the package is achieved. Alternatively in some cases a soft flexible coating is employed to reduce excessive stresses on the internal parts. Another problem that has attracted considerable attention is the possible thermal mismatch that may occur at the solder joint between package and substrate Figure 1.14a, and 1.14b. Analysis of the strain induced in the solder joints between the package and the board has led to acceptable levels of stress for temperature controlled environments.

1.7 METHODS OF THERMAL ANALYSIS

The various examples described above serve to emphasize the complexity of the heat transfer process from the silicon die itself to the ultimate thermal sink. Therefore the need for a thorough understanding of the heat transfer mechanism involved, is the only way an efficient thermal design will emerge. Because of the difficulties involved in experiments on the miniature package an accurate theoretical model is invaluable for predicting the thermal behaviour of electronic systems. A system designed in the absence of good thermal analysis, may result in undermining aspects of quality, cost, reliability, performance, and ultimately result in catastrophic failure. To satisfy the theoretical models and their limitations, a great deal of attention has been focused on

the development of numerical methods for thermal modelling. With advances in both hardware and software, many software packages exist as tools for modelling a range of thermal problems. The most common numerical techniques available for predicting the temperature distribution of electronic systems are:-

(i) Thermal resistance network
(ii) The finite difference method (FDM)
(iii) The finite element method (FEM)

Extensions of the above methods include computational fluid dynamic (CFD), packages that deal with both temperature distribution and fluid flow predictions, (conjugate flow problems).

1.8 THERMAL RESISTANCE NETWORKS

Thermal models of complex systems are most simply constructed by representing the real system as a lumped-parameter network of thermal resistances. This is appropriate because of the close analogy between the processes of conduction of heat (Fourier's Law) and conduction of electricity (Ohm's Law). Individual thermal resistances may be calculated by hand and the resultant set of equations may be solved on a computer. Considerable design judgement is required to keep the number of the nodes and resistances small. However, because of the close correspondence of this method to the finite difference method (FDM), when the number of nodes becomes large a true finite difference model may be appropriate. Typical commercial packages include: CGEN, CAD-CINDA, CATS, FERO, MELTA, NETHAN, and SPICE.

1.9 FINITE DIFFERENCE METHOD

Single nodal analysis using the finite difference method was the first numerical method to be used for both steady-state and transient thermal analysis [9]. Although the basic finite difference equations are relatively simple to formulate the method is not well suited to irregularly shaped boundaries. Other limitations of this method include, the difficulty of material selection for different regions and, the lack of facility for situations other than equally spaced nodal systems. This method, although still used, appears to be losing ground to the FEM.

1.10 FINITE ELEMENT ANALYSIS

Finite element analysis is the most recent of the numerical methods to be developed. It has the great advantage that it can be used to construct realistic models of systems which have quite complex shapes. With this method the initial geometry is input either by CAD data base or by means of a pre-processor. The model is first sub-divided into elements of various shapes and sizes, the boundary conditions are imposed and then the FE model is submitted to the solution phase for solving. Finally the results from the solution are interrogated in a post-processor. Finite element packages with heat transfer facilities include: ABAQUS, ANSYS, ADINA, COSMOS, CASTOR, DYNA, MARC, NASTRAN, and many others. Most of the above packages have available one, two, and three dimensional thermal elements, as well as special types of element for specific applications. The advantages of FEA over other numerical methods include:-

1 - The facility to call different element types within the same model.

2 - The handling of irregular geometries with variable nodal spacing as well as more precise handling of curved boundaries.

3 - It offers convenient method of selecting different materials within the same model, including non-homogeneous and an-isotropic materials.

4 - Alteration of boundary condition in different parts of the model.

The use of finite element analysis as an engineering tool is becoming more and more widely accepted for the prediction of all kinds of engineering problems. The use of this method is further simplified with introduction of packages, which hide the complexities of formulating the equations of individual elements, and of assembling them into the system matrix.

1.11 METHOD OF TEMPERATURE MEASUREMENTS

The methods of temperature measurements can in general be divided into two main groups, contact methods and non-contact methods. Contact methods such as thermocouples and thermistors are easy to implement, are commercially available and are relatively cheap. Usually this method of temperature measurement is thought to be associated with some errors due to surface contact resistance, bonding mediums and in some cases they may cause errors by distributing the flow in forced convection investigations.

A recent advance in contact methods is the development of the thin film thermocouple technique (sputter coating of two dissimilar metals on the surface of the measuring

object) which avoids the above errors. This method, which is costly and difficult to apply to a miniature package, will be discussed briefly in Chapter 4.

Although non-contact methods (such as infra-red thermometry) are very accurate, they employ complicated instrumentation and are very costly. Specific requirements include line of sight access to the measuring surface and accurate knowledge of surface emissivity. In this investigation the surface temperature measurements were carried out using infra-red methods. An alternative to a commercially available infra-red scanner was designed and developed. Later this scanner was incorporated in to a research rig and accurate detailed thermal images were obtained This is discussed in details in Chapter 6.

1.11.1 SPECIAL SENSORS

Measuring the junction temperature of miniature electronic devices is difficult. The heat source is not accessible for direct temperature measurement, hence the only possible way this temperature can be measured is by means of a sensor which forms part of the device.

In nearly all commercial electronic packages such a device exists in the form of a substrate isolation diode (SID). This component is used to protect the device from sudden current surges. However, the forward biased voltage drop across the base emitter connection of the SID can be used as a temperature sensitive parameter (TSP). During the course of this research such a technique was thoroughly investigated and

a suitable electronic circuitry was designed and developed to use the SID as method of junction temperature measurement. This is discussed in detail in Chapter 4.

1.12 LITERATURE SURVEY

The literature survey presented here is not intended to be exhaustive, but rather to be representative of certain areas of heat transfer technology as applied to cooling of microelectronic equipment. The present survey revealed a number of references but largely to studies undertaken in the United States and Japan. Work published in U.K appears to be mostly concentrated on convection cooling from printed circuit boards (PCBs) mounted in cabinets.

More references are also discussed according to their relevance in different sections of this thesis. A general survey of materials used in microelectronic components is also included. Their relevant physical properties are tabulated in Appendix A1.

1.12.1 GENERAL

A number of text books are now available which describe heat transfer applied to electronic equipment; Kraus [10], Steinberg [11], Scott [12], Kraus and Bar-Cohen [13], Bar-Cohen [14]. A book dealing specifically with cooling of components in radio electronics system was prepared by Volokhov et al [15], Baum [16] presented a chapter on thermal design consideration in a general hand book on electronic packaging. Ellison [17], Tummala and Rymaszewski [18] presented a chapter on

Thermal analysis in Microelectronic Packaging Handbook.

Although the above mentioned books provide useful, background material their generality makes them of limited use for application to realistic problems. A recent bibliography of heat transfer in electronic equipment is Antonetti and Simons [19] .

1.12.2 NUMERICAL MODELLING

Finite elements analysis

The published literature on the use of finite element analysis for solving heat transfer problems in electronic equipment is rather scarce. Although the survey revealed some publications available concerning the modelling of dual-in-line packages, very few models of surface mounted components have been published. Mostafa Aghazadeh and Debendera Mallik [20] investigate the thermal performance of single multi-layer plastic quad flat pack. A finite element model of this package is discussed and the verification of their model is supported by natural convection experiments. They also measure thermal resistance by means of a thermal test chip. Hardisty and Abboud [21] constructed a quarter symmetry three-dimensional model of 16 pin DIP using the commercial FEA package ANSYS. The model reveals the complex three-dimensional heat flow patterns within the DIP. They also illustrate the variation in temperature distribution and thermal resistance with changes in convection intensity. The verification of the model is demonstrated with experiments on a purpose built scale-model of a DIP. Although this work produced valuable data, the experimental data from the scaled model is limited. Kraus et al [22] discuss the generation of a simple F.E model of a prototype avionics power supply, but no details are included.

Resistance network analysis

Welling [23] illustrates a detailed model of a chip carrier mounted on printed circuit board using the thermal analyzer MELTA. The model is based on the lumped parameter approximation of the various thermal resistance paths from the chip carrier to its local thermal sink. The analysis investigates the effects of changes in carrier material, the use of a ground plane in the PCB, and the effect of using a conduction backup plate. Few details of the chip carrier model are given, and there is no evidence of the die-bond material investigation. Also the thermal resistance path between the base of the carrier and the top convective surface is ignored.

Mitchell and Berg [24] illustrate the construction of a simple lumped-parameter network model of a 16 pin DIP. Even though the model provides comparative information concerning the effects of the different materials used, in order to establish and quantify the complex three dimensional heat flow patterns within the DIP, a more detailed analysis would be required. The need for a more refined thermal model of a chip carrier is outlined by Maclaughlin et al [25]. More investigation of die-bond and non-wetted bond areas are required, to demonstrate the additional temperature rise effects.

1.12.3 SURVEY OF COOLING METHODS

Although the cooling scheme selected for a given design depends on many factors such as cost, operating environment, and available space, the two key factors which dictate the thermal design are heat flux and the permitted device temperature rise

above the local coolant temperature. Figure 1.5 presents the application range of various cooling schemes as a function of package to coolant temperature difference versus power levels per unit area. From Figure 1.15, it can be seen that natural convection and radiation are appropriate only for cooling systems with very low heat dissipation and low temperature differences, of the order 60 deg c. However if forced convection is employed as the cooling method, the flux can almost be doubled. Immersion cooling with pool boiling does however offer dramatic advancement in the transferable heat flux even at a temperature difference as low as 20 deg c [26]. Direct air cooling remains one of the most common methods employed for the cooling of micro- electronic equipment. This method of cooling is very attractive due to low cost, ease of implementation, and good performance. This review mainly concentrates on forced convection air cooling methods, however references [27-29] refer to natural convection cooling methods.

In heat transfer by forced convection, a fan or a pump is used to provide high velocity fluid flow (air/liquid) past a heated surface. The high velocity fluid results in a decreased thermal resistance across the boundary layer from the fluid to the heated surface. This in turn increases the amount of heat that is carried away by the fluid. In a study of forced convection cooling of a uniformly heated array of electronic devices mounted on printed circuit board by Wills [30] presents an empirical formula for the heat transfer coefficient at any stream-wise location along the PCB. The proposed simple lumped parameter resistance heat transfer model is based on an expression for fin efficiency Wills [30] further analyses the non-uniform heating of PCBs. Here his initial procedure is modified by using empirically derived influence coefficients to

estimate the effect of heated wakes from upstream powered modules on the temperature of other modules downstream.

Based on their experimental measurements Hardisty et al [31] proposed an empirical heat transfer correlation of forced convection cooling of an array of resistor pack (DIPs) mounted on multi-layer printed circuit boards. Their work was supported by FEM thermal modelling of the DIPs. However their temperature measurements using thermocouple attached to the DIP were somewhat limited, and the test rig used for experimental investigation had a transition area that may have caused a flow disturbance which affected the boundary layer development.

Moffat et al [32] present an experimental study of forced convection related to the thermal protection of individual elements in an air cooled array of electronic components. Heat transfer coefficients and thermal wake functions, are presented for an in-line array of cubical elements mounted on one wall of a parallel plane channel. Several combinations of channel widths and approach velocities were used. The hydrodynamic data show that when the channel height is large the bulk of the fluid passes over the elements without interaction and makes little or no contribution to the cooling. The work presented is only applicable to elements of large height and is not applicable to flat-packs. The theory concerning the thermal wake effects was developed for modules mounted on an non-conducting, adiabatic substrate.

Parkes and Preston [33] outline the difficulties involved in predicting the heat transfer coefficient for fan cooled systems. These depend on the arrangement of the packages

on the PCB, the overall physical lay-out of the system, and the number and the type of fan used. Their experimental data was verified by means of a lumped resistance network model of a DIP. By using the finite difference solution to the Navier-Stoke equation for laminar flow, the authors attempted to predict the flow regime around a DIP.

Experiments to predict the heat transfer coefficient of electronic modules (ceramic chip carrier), were carried out by Buller and Kilburn [34]. The primary objective of the authors was the determination of the quantity of power dissipated through the module lid (cap) and hence to the air stream. The test arrangement was such that the pin of the modules was insulated. The experimental result is presented in the form of a correlation based on the Colburn j-factor.

A proposal by Finch and Goodacre [35] for the determination of the maximum junction temperature of DIPs when closely packed as an array under forced convection cooling is achieved by the use of an empirical formulae. Forced air cooling of 4 rows of PCBs each PCB containing 7 x 10 DIPs, with 5 PCBs per row, was carried out in a cabinet. The results describe the general temperature distribution in a cabinet, and the derivation of an empirical formula for uniformly powered PCBs. Unfortunately the experiment did not provide detailed temperature distribution of a single printed circuit board. Publications concerning thermal analysis of surface mounted components are scarce, and few appear in the open literature.

1.13 BACKGROUND TO EXPERIMENTAL MEASUREMENTS PROBLEMS CONSIDERED

1.13.1 GENERAL

The theoretical and experimental research presented in this thesis is concerned with the complex three dimensional heat transfer involved in an electronic package mounted on printed circuit board.

The heat transfer problem may be described as a combined conduction and convection model. The generated heat in the chip is initially conducted to the flag (in case of DIPs) which acts as a heat distributor to other parts of the package. The heat is then conducted through the leads to the PCB and encapsulant to the external surfaces of the package. Forced or natural convection used to cool the package constitutes the external resistance.

Initially the principal aims of the investigation were as follows:-

1) To design and develop an accurate method of junction temperature measurement.

2) to design and develop an alternative to commercially available infra-red scanning system to carry out accurate non-contact surface temperature measurement.

3) To determine the convective heat transfer coefficient on the outer surface of the package.

The attainment of all of these objectives is made difficult by the miniature nature (and large number) of the packages under investigation.

In previous research at Bath, package temperature had been monitored by a small

thermistor glued into a convenient recess on the under surface of the DIP Figure 1.16. It will be apparent that this method is unsatisfactory in that neither the temperature of the chip (the maximum temperature) nor the temperature on the upper convective surface (necessary to determine h) is directly measured.

1.13.2 JUNCTION TEMPERATURE MEASUREMENT

The silicon chip is encapsulated within the package and is not accessible by conventional methods of temperature measurement. To overcome these difficulties a novel method of temperature measurement was implemented and developed in this research.

One of the electronic components on the chip itself the, Substrate Isolation Diode (SID), was used as a resistance thermometer to measure the junction temperature. Because silicon is a relatively good thermal conductor, this temperature is closely representative of the chip temperature itself. Of course, before the SID could be used as a resistance thermometer, its temperature/resistance characteristics had to be established. Also a suitable electronic high speed switching circuit to detect this resistance during normal operation of the chip had to be designed. A detailed account of this development is given in Chapter 4.

1.13.3 SURFACE TEMPERATURE MEASUREMENT

Initially the feasibility of sputtering two dissimilar metals on the surface of a DIP was investigated (thin film thermocouple). Although the method was successful in principle it was not feasible due to cost and time constraints. For this investigation the infra-red was then considered. The commercially available infra-red scanners are very costly, as a consequence the design of a mechanical scanner was considered. With comprehensive software and hardware development, a static infra-red thermometer was made to traverse an X-Y plane in controllable steps over the object to obtain a temperature array file. The temperature array file obtained from the X-Y traverse readily converts the pixel temperature to a thermal image using the image program developed in this research. The scanner was later incorporated into the research rig.

Systematic experiments accompanied by realistic finite element models was then carried out to evaluate the heat transfer coefficients over uniformly and non-uniformly powered printed circuit boards with an array of DIPs and SMCs. The use of the above methods of temperature measurements assisted by FE models also made it possible to carry out steady-state and transient analysis of DIP, chiprack, and PLCCs (20 pin plastic leaded chip carrier)

1.14 RESEARCH BACKGROUND AND OUTLINE OF THESIS

The origin of this research at Bath was in the early 1980s, when an industrial request was presented to the supervisor of this thesis. This enquiry concerned the feasibility

of using the FEM to analyze the thermal performance of electronic systems.

The objective of this research was to carry out an accurate experimental and finite element investigation to complement previous theoretical FE research. In addition to making significant changes in the experimental methodology, new techniques of temperature measurement were developed and used for both steady-state and transient thermal analysis. This thesis is divided into eight chapters; general remarks and background to the investigation are set out in chapter (1), which also contains relevant previous work. Chapter (2) is subdivided into two parts; part one outlines a background to finite element theory, and part two provides an insight into the use of the ANSYS FE package. Chapter (3) initially gives a detailed assessment of the existing research rig for accurate thermal analysis. This rig was modified and then used to investigate the heat transfer coefficient correlation over uniformly powered DIPs cooled by impinging jets, at task for which it was suitable for. Chapter (4) details the design and development of complex fast electronic circuit to forward bias and measure the voltage drop across base emitter connection of an isolation substrate diode, which is representative of the junction temperature. The SID method accompanied by a realistic theoretical FE model, is then used to analyze the steady-state and transient thermal performance of a 14 pin DIP.

Using the junction temperature measurement technique Chapter (5) provides theoretical FE model and experimental steady-state and transient study of a novel chip carrier (chiprack) designed and developed by Dowty Electronics. Chapter (6) describes the design and development of the forced convection cooling test rig and an infra-red

mechanical scanner for surface temperature measurement. The method was used to predict the heat transfer coefficient over uniformly and non-uniformly powered DIPs. Chapter (7) details the design and development of a custom made printed circuit board with an array of surface mount components (20 pin PLCC package). The circuit board was initially used to deduce the conductivity of the plastic encapsulant using experiment and combined FE, IR method. Heat transfer correlation of the uniformly powered PLCCs is also under taken. Finally Chapter (8) concludes the present study.

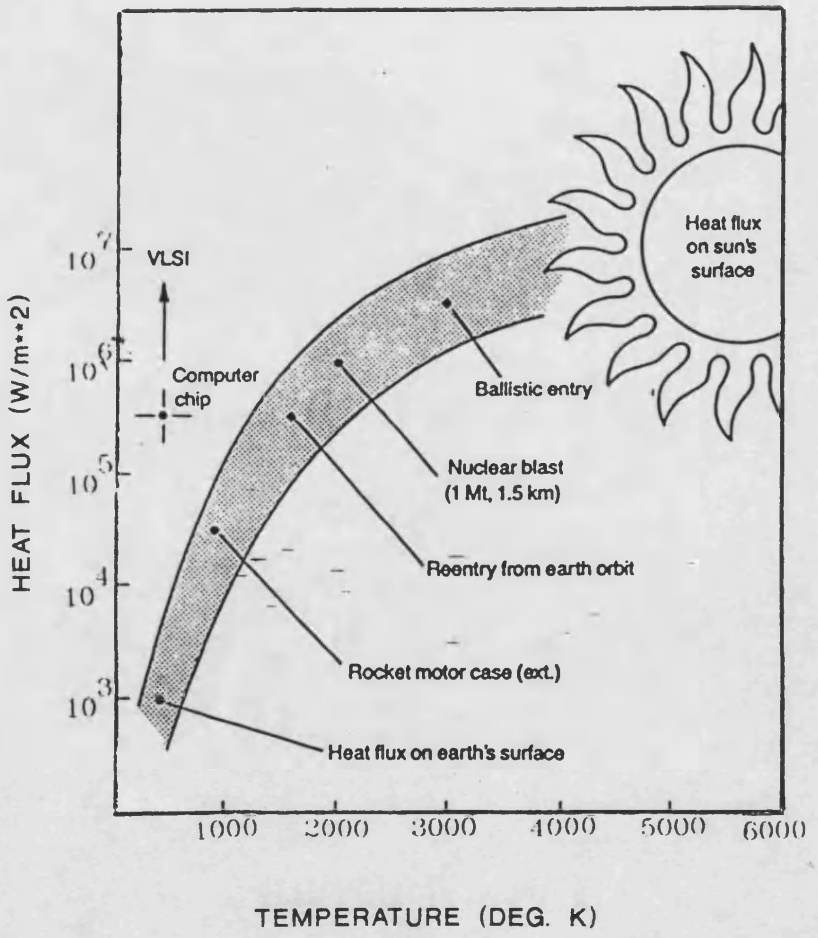


FIGURE 1.2a -
HEAT FLUX COMPARISON OF SEMICONDUCTOR PACKAGES

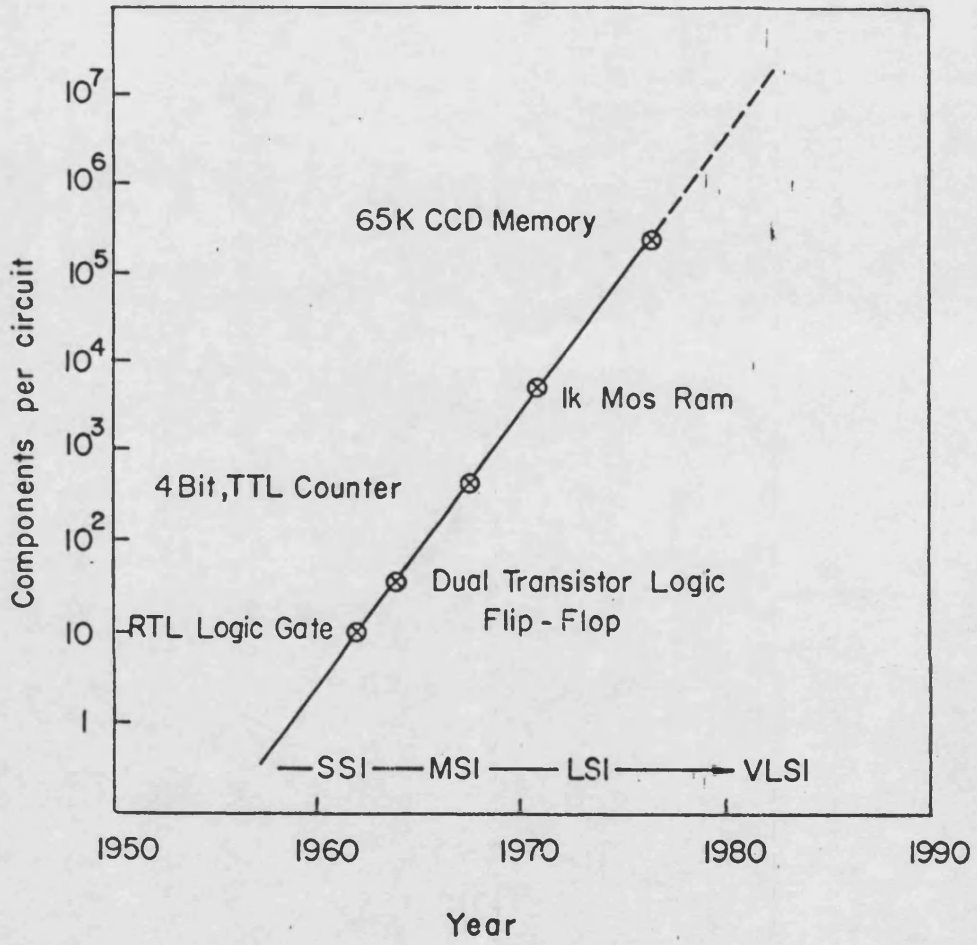


FIGURE 1.1 -
STATE OF THE ART IN CIRCUIT COMPLEXITY

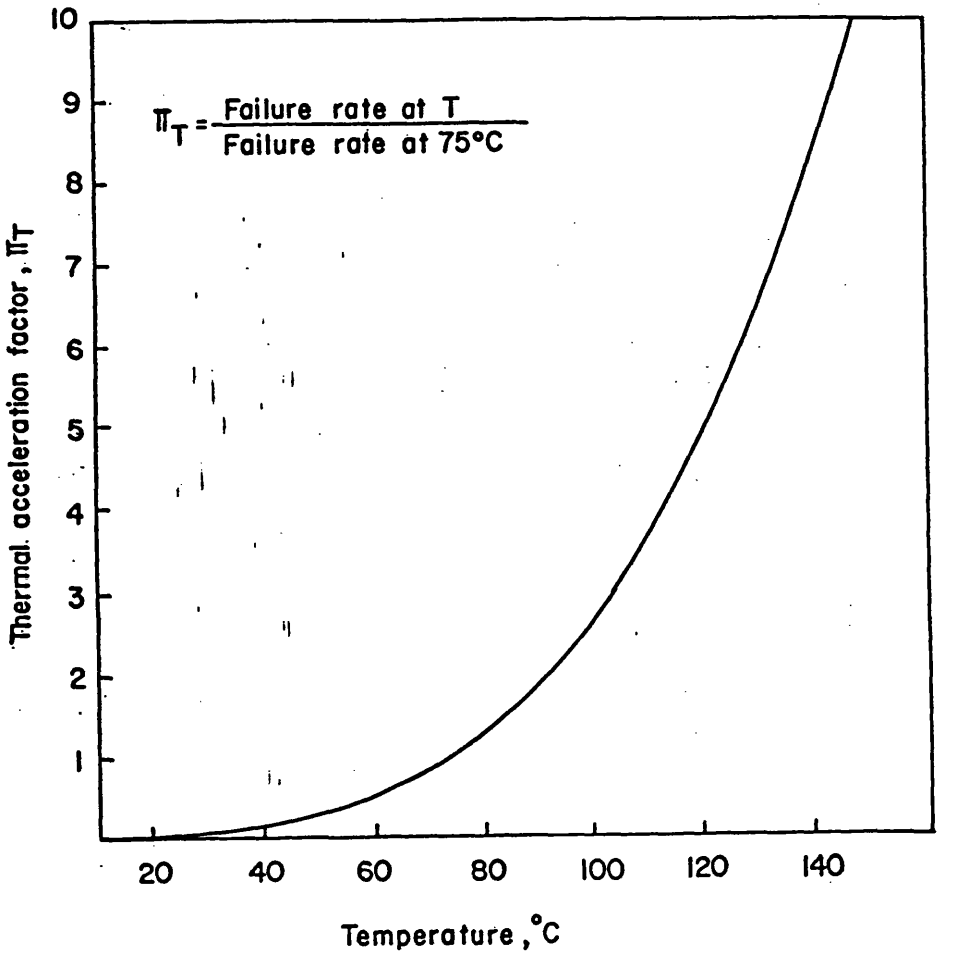
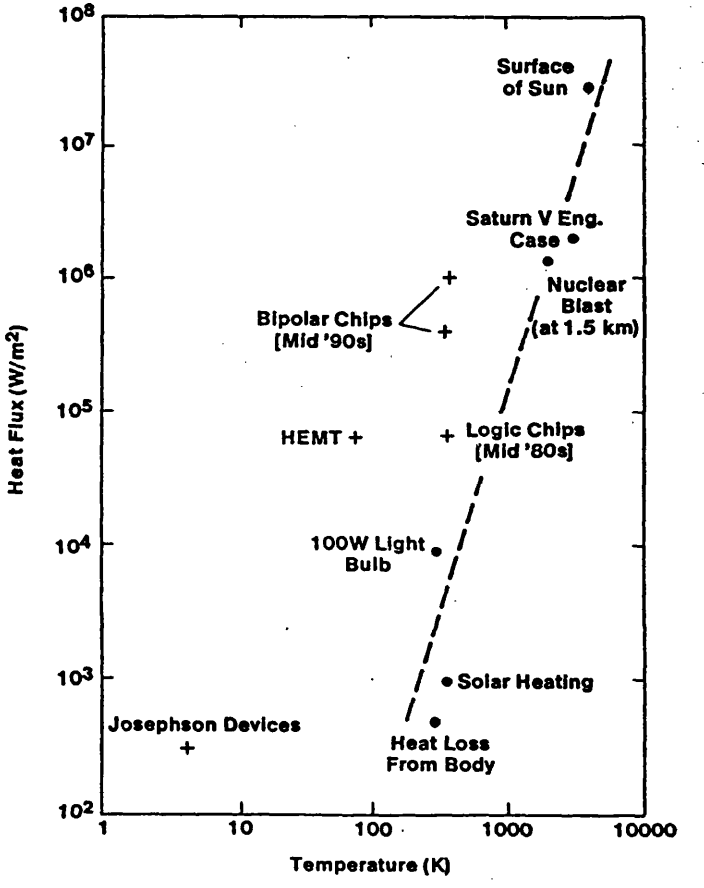


FIGURE 1.3 -
THERMAL ACCELERATION FACTOR FOR BIPOLAR DIGITAL DEVICES



GURE 1.2b -
HEAT FLUX VS TEMPERATURE LEVEL

LARGE HIGH-PERFORMANCE COMPUTERS REQUIRED MANY GATES

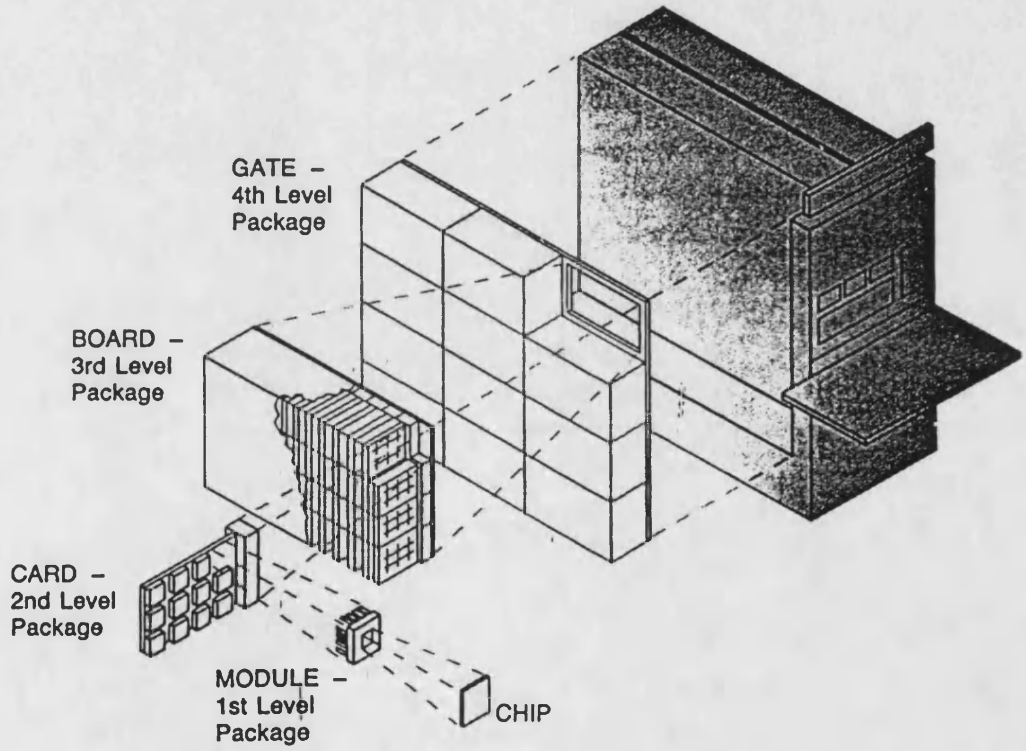
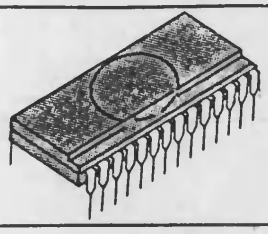
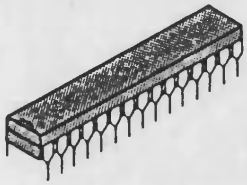
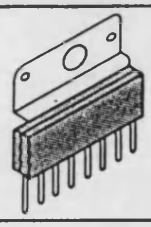
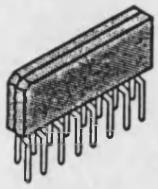
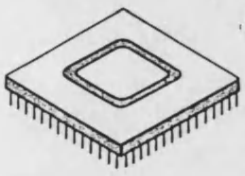


FIGURE 1.4 - ELECTRONIC PACKAGE HIERARCY

Through Hole Package

a		DIP(Dual In-line Package)
b		SH-DIP (Shrink DIP)
c		SK-DIP SL-DIP (Skinny DIP, Slim DIP)
d		SIP (Single In-line Package)
e		ZIP (Zig-zag In-line Package)
f		PGA (Pin Grid Array)

Surface Mounted Package

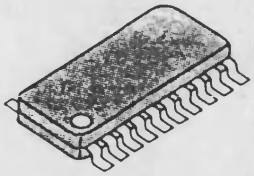
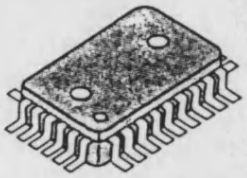
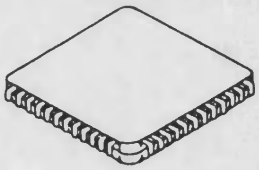
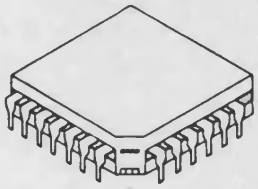
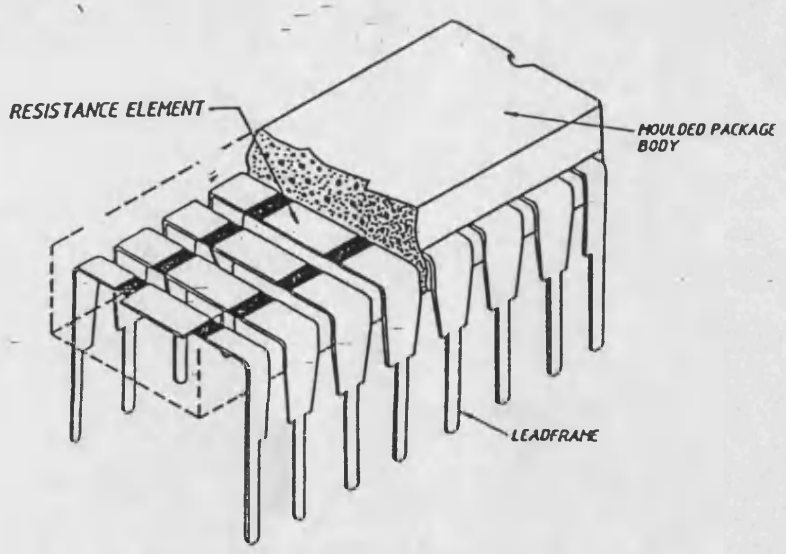
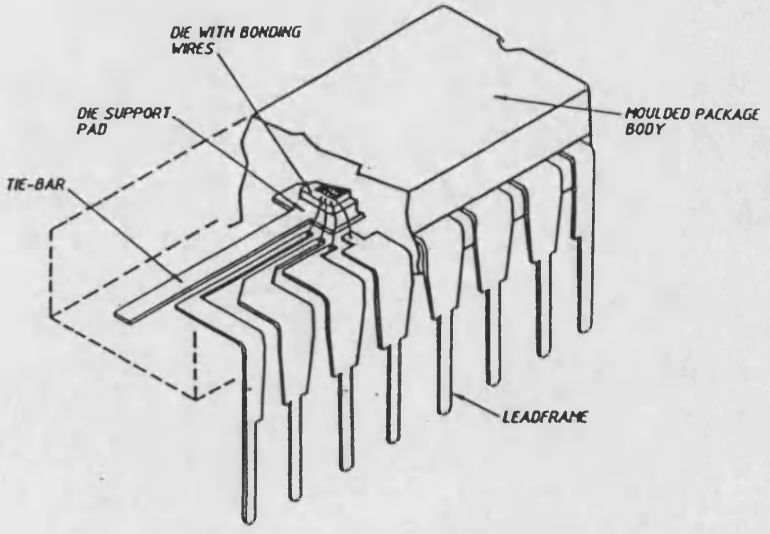
g		SO or SOP (Small Out-line Package)
h		QFP (Quad Flat Package)
i		LCC (Leadless Chip Carrier)
j		PLCC SOJ (Plastic Leaded Chip Carrier, Small Out-line J-lead Package)

FIGURE 1.5 - SMT AND PTH PACKAGES



TYPICAL DIP RESISTOR PACK



TYPICAL DUAL-IN-LINE PACKAGE

FIGURE 1.6a - INTERNAL CONSTRUCTION OF DIP

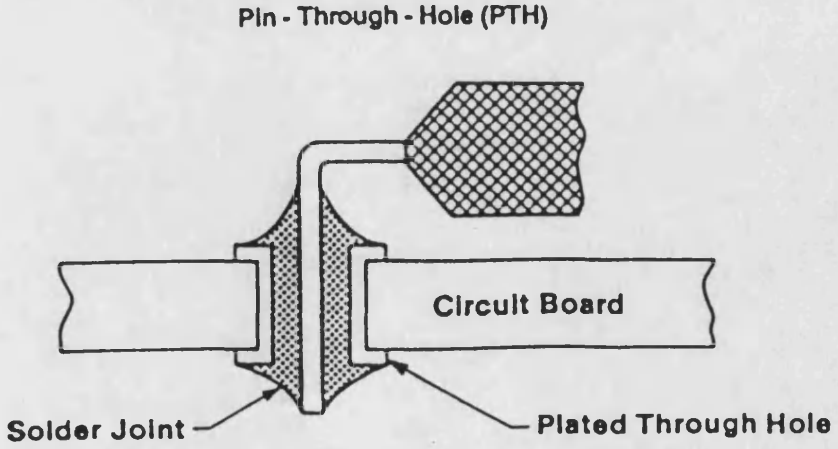


FIGURE 1.6b - SOLDER JOINT OF DIP

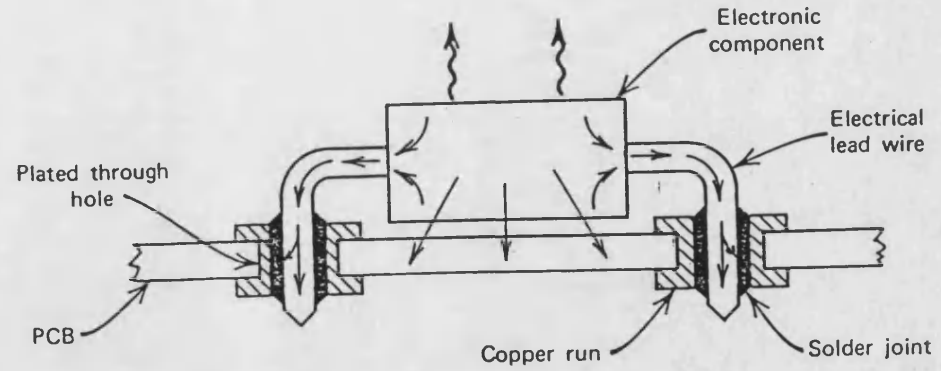


FIGURE 1.7 - HEAT CONDUCTION PATH OF PACKAGE

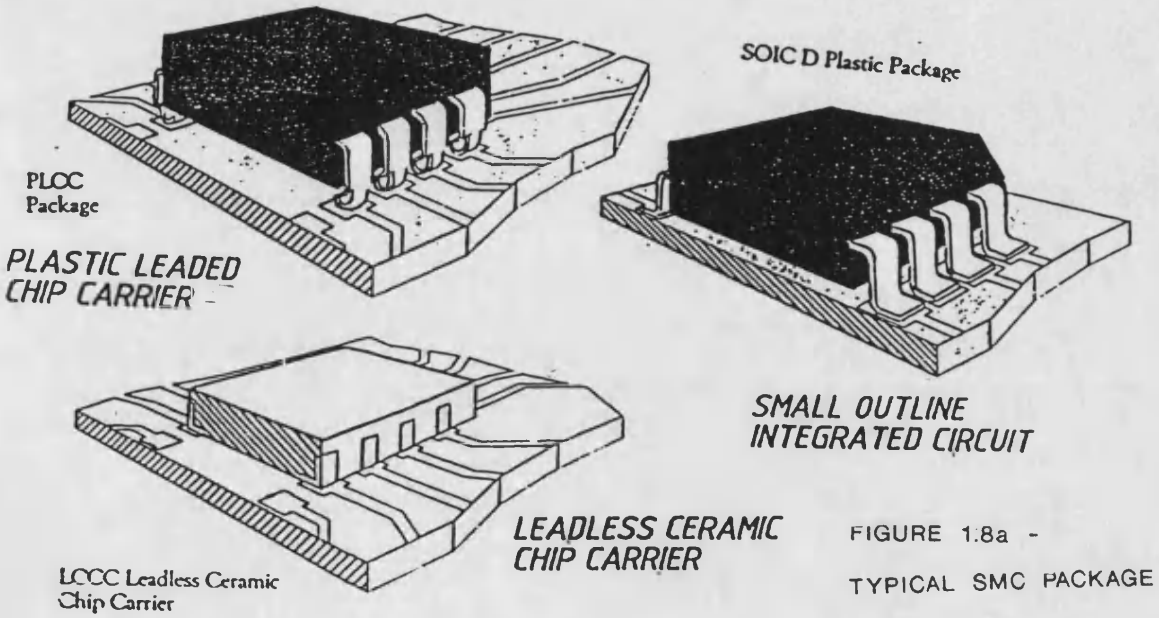


FIGURE 1.8a - TYPICAL SMC PACKAGE

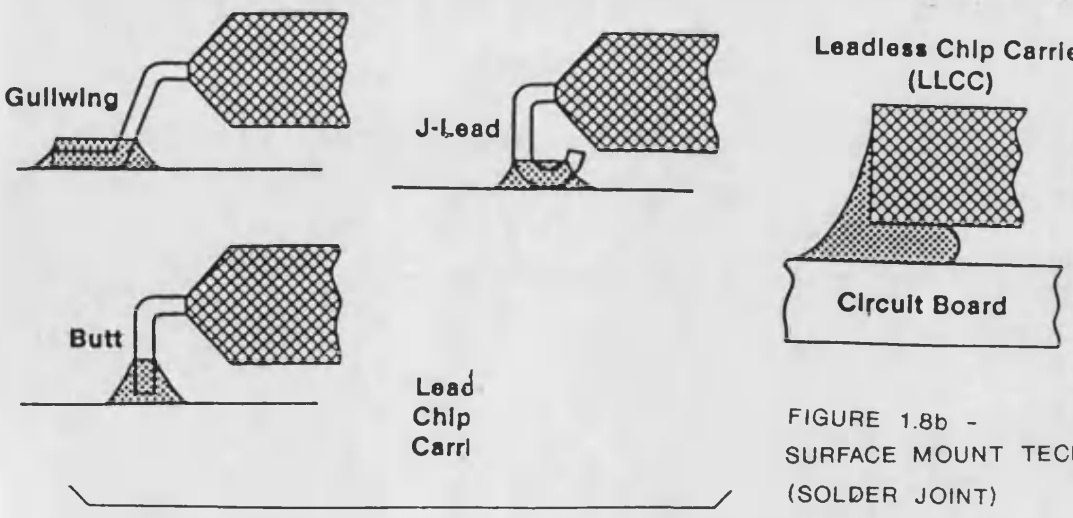
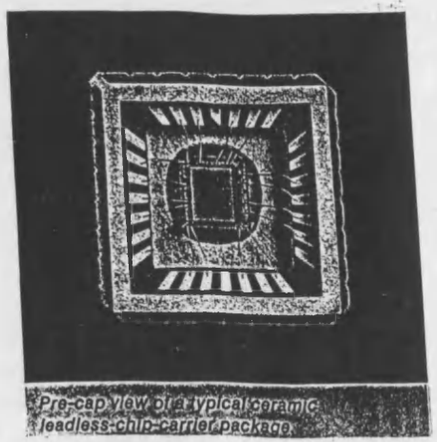
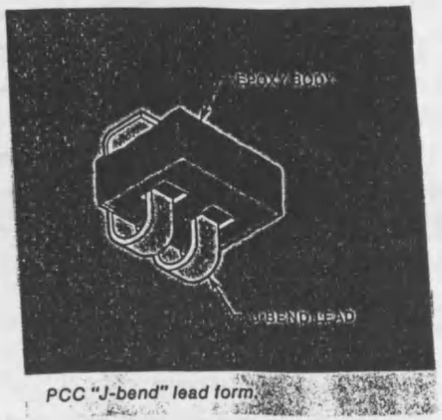


FIGURE 1.8b - SURFACE MOUNT TECHNOLOGY (SOLDER JOINT)

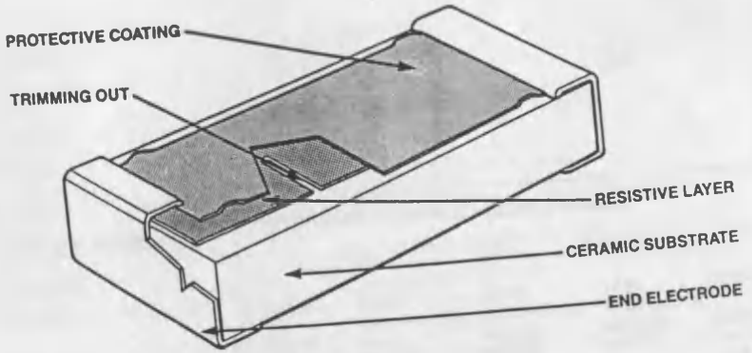


Pre-cap view of a typical ceramic leadless-chip-carrier package.

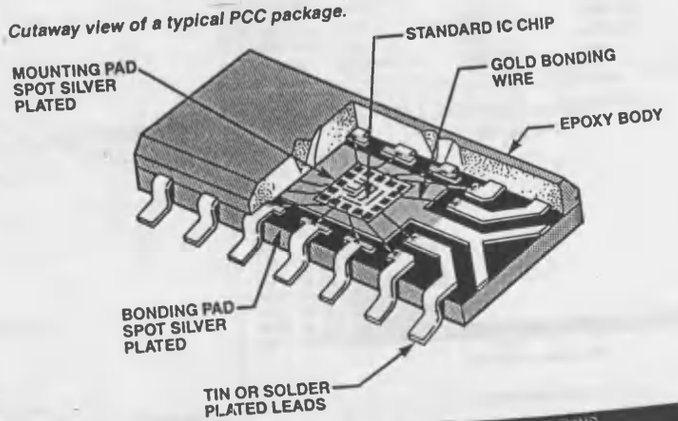


PCC "J-bend" lead form.

FIGURE 1.9b -
TYPICAL CUT AWAY VIEW OF SMD LEADS



Cutaway view of a typical PCC package.



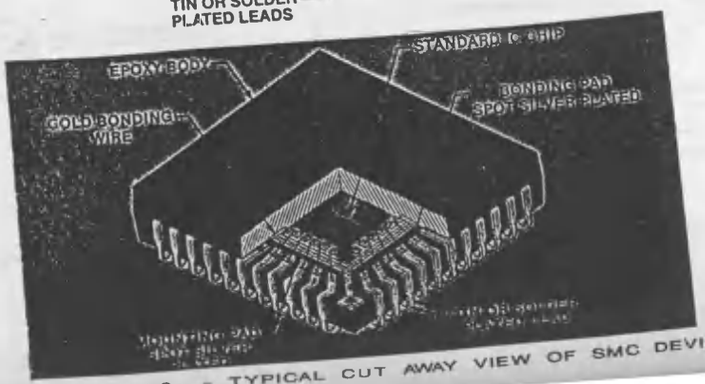


FIGURE 1.9a - TYPICAL CUT AWAY VIEW OF SMC DEVICES

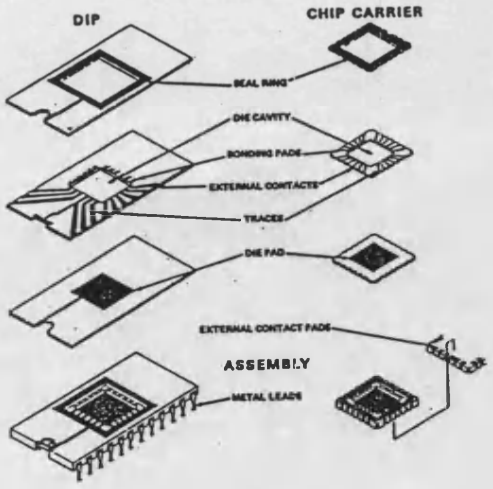


FIGURE 1.11b - EXPLODED VIEW OF CHIP CARRIER AND DIP

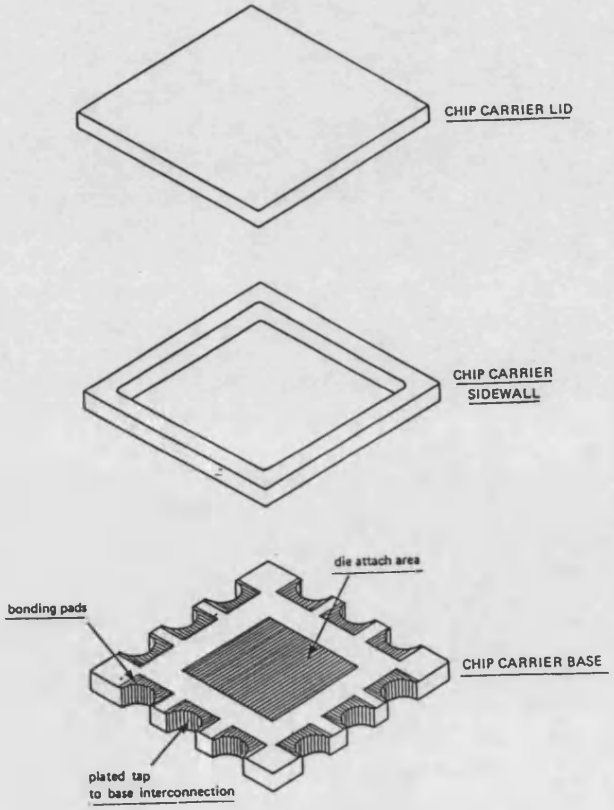


FIGURE 1.11a -
EPIC CHIP CARRIER CONSTRUCTION

Comparison of surface mount packages

	SO	QFP	PLCC/SOJ	LCCC
Pin count	8 to 28	36-164	18-84	18-84
Size	optimum < 28	optimum > 44	optimum > 28	
AC perf.	good	optimum	optimum	optimum
Board	std PCB	std PCB	std PCB	spec.mat.
Routability	good	poor	poor	poor
Visual insp.	easy	easy	difficult	difficult
In circuit test	easy	easy	difficult	difficult
Socketing	difficult	difficult	easy	easy

Through hole/SMT packages comparison :

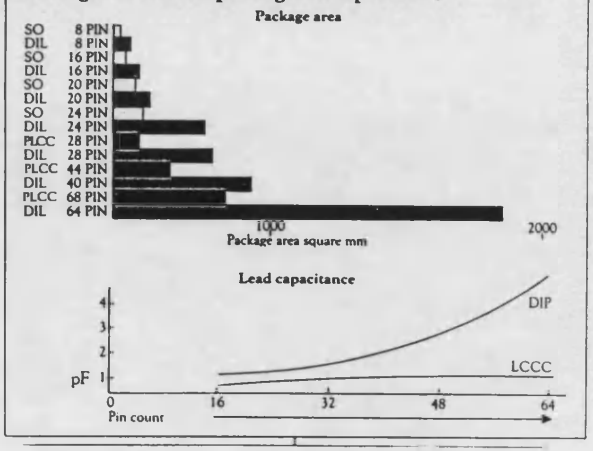


FIGURE 1.10 - SIZE COMPARISON OF SMC AND DUEL-IN-LINE PACKAGES

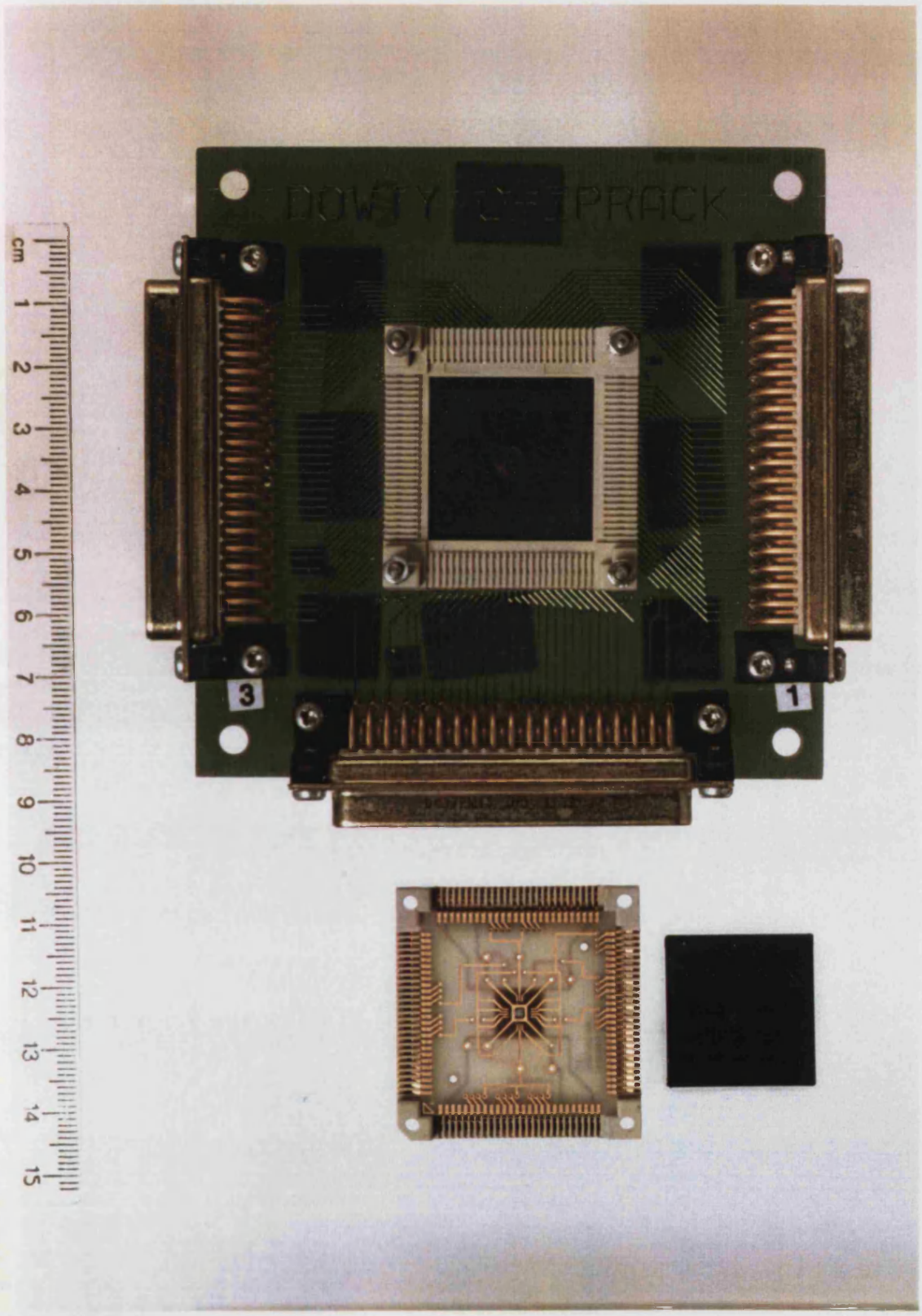


FIGURE 1.12a - CHIPRACK ASSEMBLY

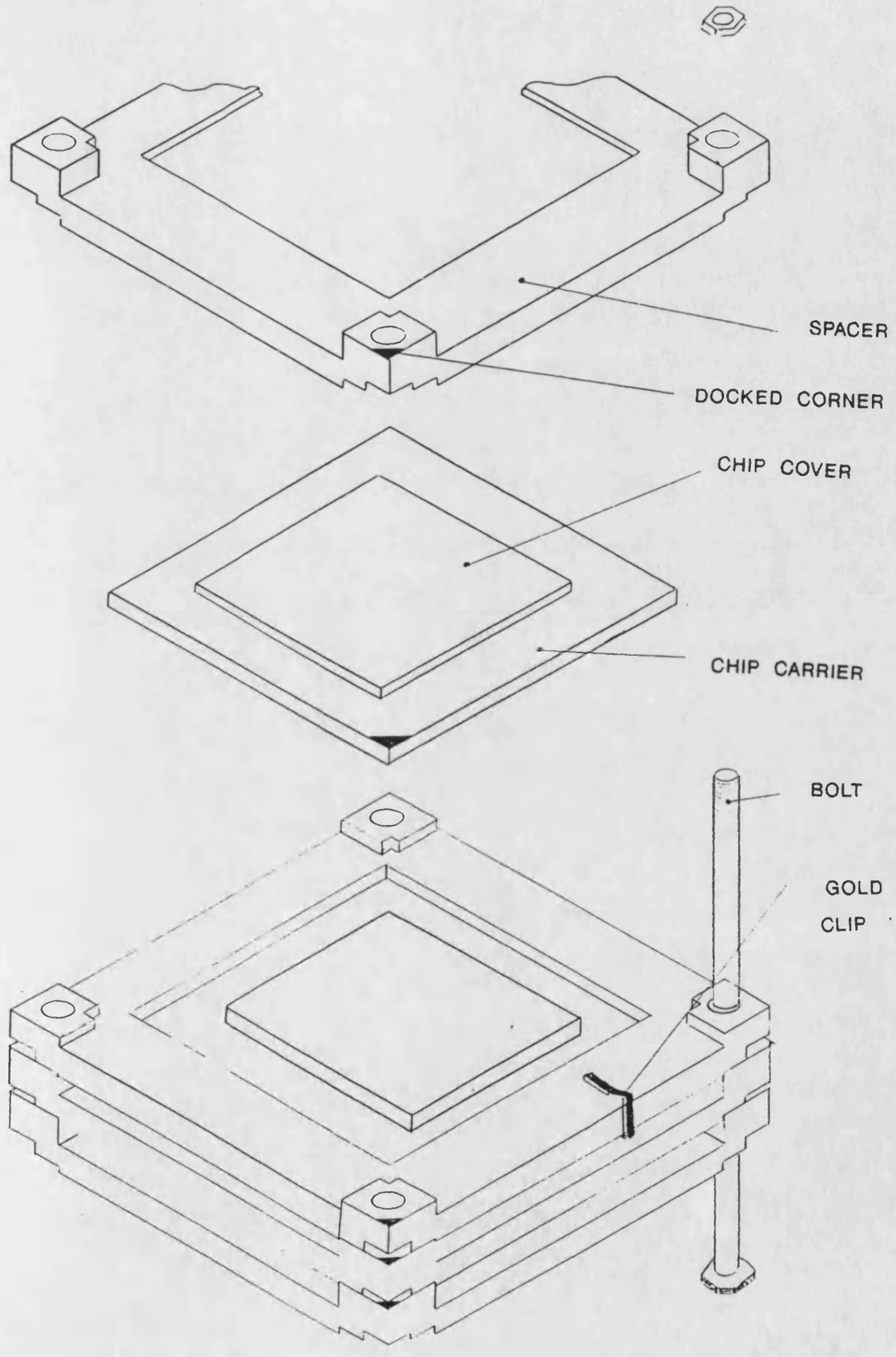


FIGURE 1.12b - LEVELS OF CHIPRACK

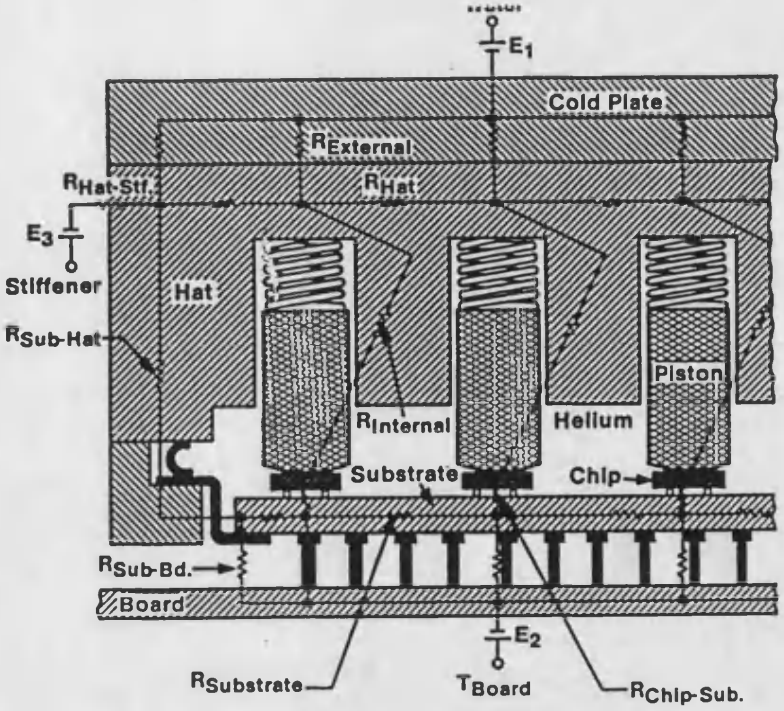


FIGURE 1.13a - IBM THERMAL CONDUCTION MODULE

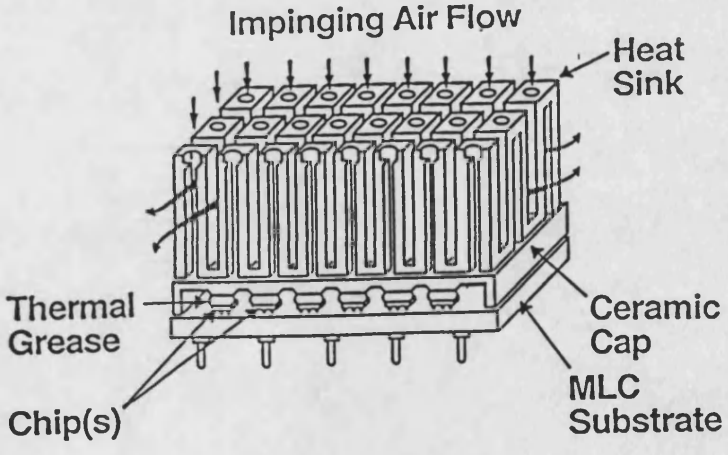


FIGURE 1.13b - IBM 4381 AIR-COOLED MODULE

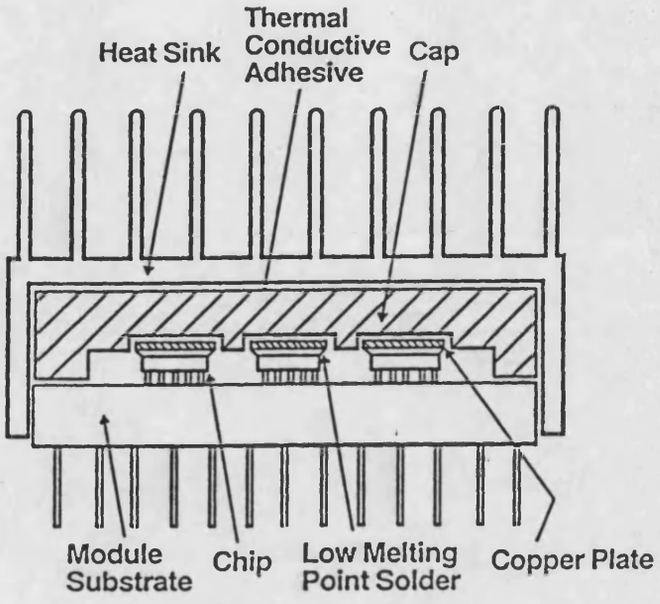


FIGURE 1.13c - MITSUBISHI HIGH THERMAL CONDUCTION MODULE

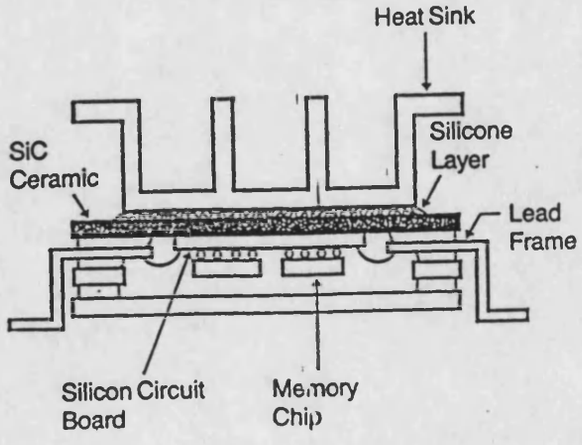
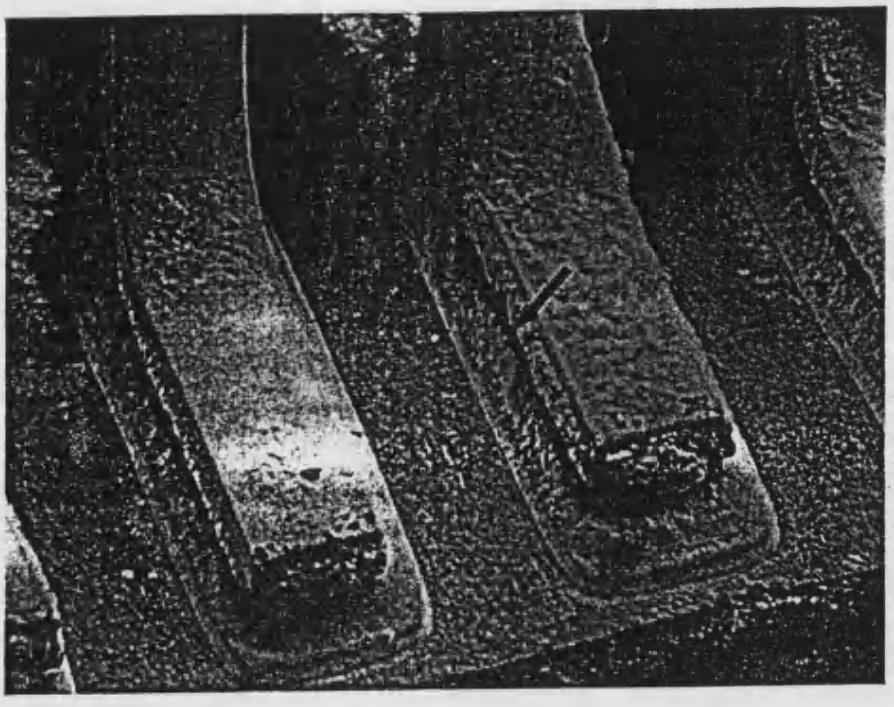
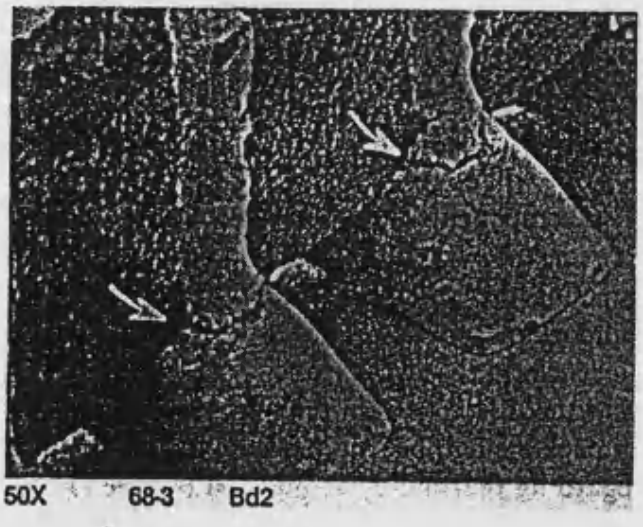


FIGURE 1.13d - HITACHI SILICON-CARBID RAM MODULE



Solder Joint Failures. a) Cracking of the solder joint under thermal fatigue cycling in a Gullwing SOIC. b) Cracking of the solder joint under thermal fatigue in leadless chip carrier.

FIGURE 1.14a -



Cast Solder Column Interconnections. The solder columns are prepared using spherical solder preforms, which are cast into mold cavities adjacent to the I/O contact pad. The mold is removed and the package is surface soldered to the circuit board.

FIGURE 1.14b -

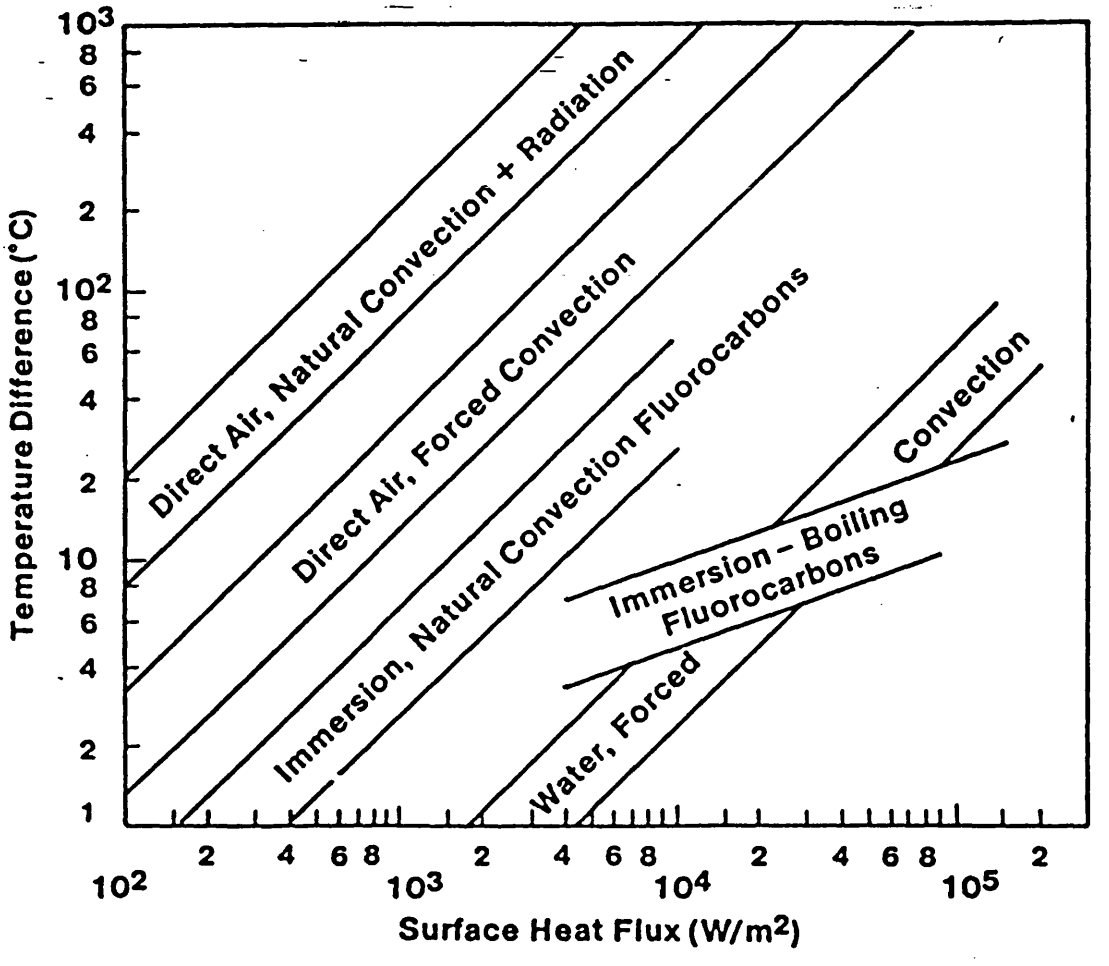


FIGURE 1.15 - TEMPERATURE DIFFERENCE VS SURFACE HEAT FLUX FOR VARIOUS COOLING

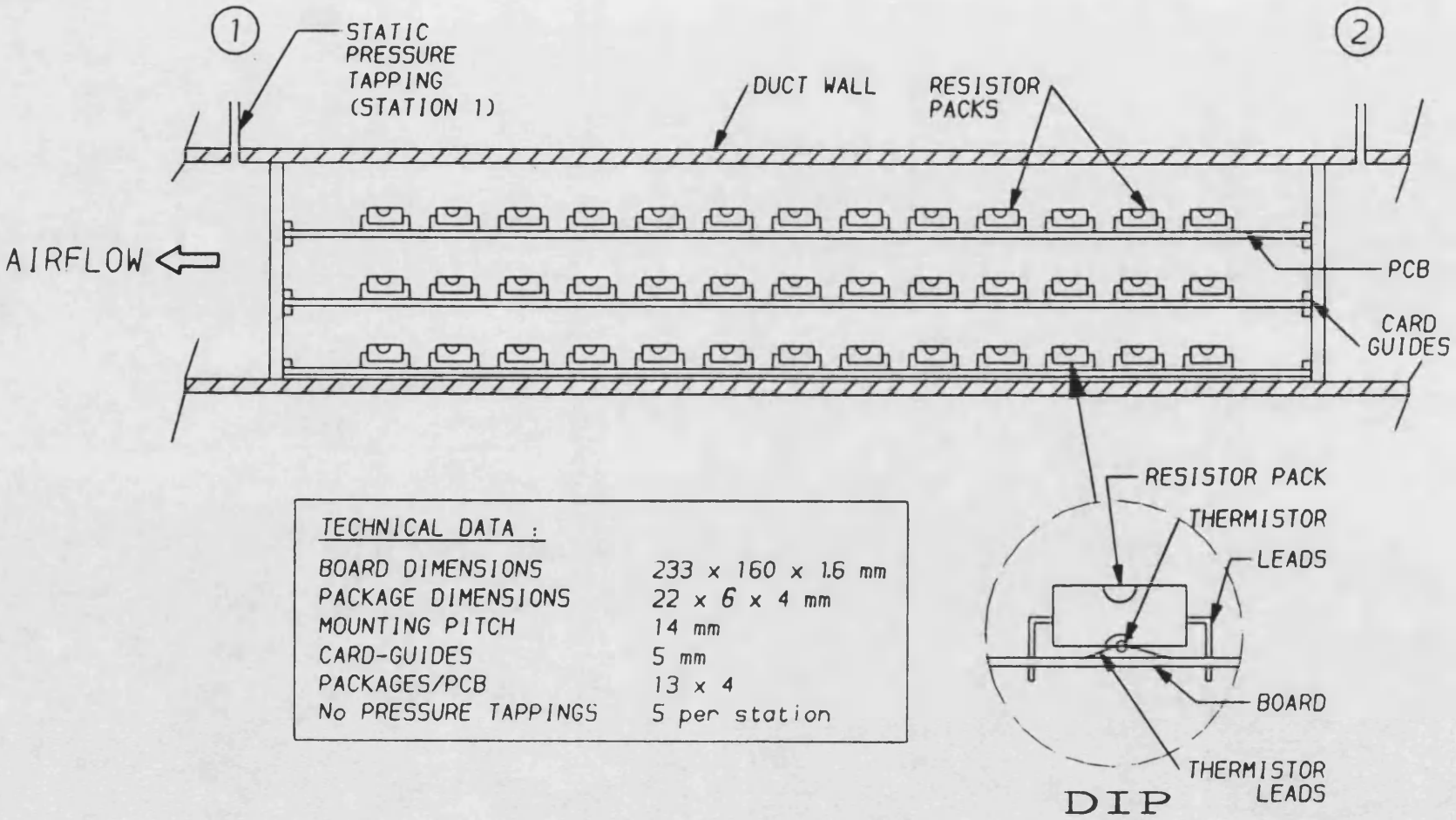


FIGURE 1.16 - TEST SECTION OF RESEARCH RIG

CHAPTER 2

THE FINITE ELEMENT METHOD

PART I FINITE ELEMENT BACKGROUND AND THEORY

2.1 INTRODUCTION

The response of most real-world engineering systems to applied action is usually difficult, if not impossible, to determine by a closed-form mathematical solution. However, there are two common numerical methods which offers a convenient way of obtaining approximate solutions to most engineering problems.

1) Finite difference method (FDM)

2) Finite element method (FEM)

Early numerical algorithms predominantly used the finite-difference method to solve differential equations. A finite difference model of a system involves dividing the domain into a grid of discrete nodes. Difference equations are written for each node such that derivatives are replaced by finite differences. Although approximation based on this method is relatively easy to understand, it has a number of limitations. In particular, it becomes difficult to apply to systems with irregular geometry, unusual boundary conditions, or non-homogeneous composition.

The finite element method (FEM) is widely regarded as the more powerful method of the two for the solution of continuum problems in physics and engineering. The basic concept of FEM is that the structure to be analyzed is considered to be an assemblage of discrete pieces, called elements, that are connected together at a finite number of

points or nodes. Each node has a degree of freedom (DOF) which in the case of thermal analysis is the temperature of the node.

For a thermal analysis, having represented the structure by two- or three-dimensional elements, the temperatures within the element are related to the temperatures of the nodes by a temperature or interpolation function. A conductivity (stiffness) matrix, which relates the nodal temperature of an element, is a combination of the temperature function and material properties of the element. By imposing equilibrium (a heat balance) at every node, the individual element conductivity matrix (element matrices) are assembled into a set of linear simultaneous equations. This equation set is solved for the nodal temperatures, from which quantities such as thermal gradients can be obtained.

2.1.1 THE FINITE ELEMENT METHOD IN ELECTRONIC COMPONENT FOR DESIGN AND ANALYSIS

In the past, designers have used classical analysis techniques. These, although useful for rough predictions for simple components, are totally inadequate for analysis of modern electronic system such as the temperature distribution in an electronic package or the induced stresses due to thermal mis-match. Hence, the traditional approach to a new system was to design it using traditional techniques and to rely heavily on testing. The failed components were redesigned and retested. After the advent of high speed computers, complex electronic systems could be simulated using techniques such as the finite element method. In this investigation the powerful feature of the FE

method was explored by construction of realistic FE models, including all the details that may effect the thermal performance of the electronic package

The overall objective of FE thermal analysis is to help and ensure the overall 'integrity' of the design, before prototype manufacture and testing. Although it would be ideal to incorporate the complete electronic system during an analysis, certain simplifications must be accepted.

2.2 HISTORICAL PERSPECTIVE

The roots of the modern day finite element method (FEM) developed around the turn of this century with the use of lattice analogy to solve solid continuum structural problems. With this technique, the structure was divided in to a regular mesh of elastic beams. Beam theory was then used to approximate the true solution of the structure.

In the early 1940's a mathematician named Courant [36] suggested a Rayleigh-Ritz approach where the structure is divided into triangular subregions. Motivated by Euler's publication [37], Courant described each subregion by polynomial functions to approximate the exact solution. However the practicability of Courant's method was limited because there were no digital computers to do the tedious calculations. By 1953 with the introduction of digital computers that could solve large simultaneous equations, the now feasible matrix methods became popular in engineering circles, especially in the aerospace industry.

Interest in FEM increased dramatically in 1956 with a publication by Turner, Clough, Martin and Topp [38], in which the actual solution of plane stress problems by means of triangular elements whose properties were determined from the equations of elastic theory was given. Although there was some limited use of FEM in heat transfer and fluid flow problems, the use of the method in the 1960s was mainly limited to structural analysis. In 1965, Zienkiewicz and Cheung [39] reported that the finite element method is applicable to all field problems which can be cast into variational form.

The introduction of the Frontal Solution Algorithm by Irons in 1970 made the equation solving phase of the technique more adaptable to a wider variety of hardware. In 1971 Zienkiewicz wrote the first fundamental text book on the subject [40].

Large, general purpose finite element programmes emerged during the late 1960's - early 1970's period. These general programmes combined the special features of many small programs into analysis packages.

The finite element code ANSYS (used in this research) was introduced by Swanson Analysis Systems, Institute (SASI) in 1970, gave analysts the capability to perform static, dynamic and heat transfer calculations in a single program.

The proliferation of superminis with interactive operating systems and graphics terminals also brought about changes in the FE codes. The codes had to be

reconstructed for use in an interactive environment. In the case of the ANSYS program the solution modules were maintained as basically batch operations. However, data preparation preprocessing and results evaluation (postprocessing) were created to be used interactively.

In 1985, SASI put finite element technology within the reach of most engineering firms when it introduced derivatives of the ANSYS program to personal computers.

2.3 THE METHOD

The name finite element summarises the basic concept of the method. The transformation of an engineering system with infinite number of unknowns (the response at every location in a system) to one that has a finite number of unknowns related to each other by elements of finite size. The unknowns, called degrees of freedom, represent the responses to applied actions. Typical degrees of freedom with corresponding actions and applications are listed in Table 2.1.

TYPE OF DEGREE OF FREEDOM	ACTION	APPLICATION
Displacement	Force	Structural
Temperature	Heat flow rate	Heat transfer
Volt	Current	Electrical
Magnetic potential	Current	Magnetic
Pressure	Fluid flow rate	Fluid flow

Table 2.1 - The degrees of freedom, actions and applications

The degree of freedom and the actions are related by a set of basic equations. The purpose of the finite element method is to determine the solution to these across the

entire engineering system being analyzed. The simplest form of a basic equation is as follows;

$$[K]\{d\} = \{A\}$$

Where {d} is the degree of freedom vector, {A} is the action vector, and [K] is the matrix relating {d} to {A} (often called the stiffness or coefficient matrix). In general [K] and {A} are unknown, and {d} is initially unknown. The actual form of a basic equation is determined by type of analysis being performed, for a steady-state thermal analysis, the equation is:-

$$[K]\{T\} = \{Q\}$$

Where [K] is the thermal conductivity matrix, {T} is the temperature vector, and {Q} is the heat flow rate vector.

In order to solve the basic equation across the entire engineering system, the system must be represented (modelled) by discrete, interconnection pieces (elements). Once the [K] is determined for each element, all of the individual [K] matrices are assembled to form the set of simultaneous equations. Solution of the simultaneous equations gives response values at every degree of freedom across the entire system.

The execution of the finite element method usually follows a step-by-step procedure parts of which may be invisible to the user if a modern packages is used. The following list describes the steps involved.

1 Model characterisation (1-d, 2-d, 3-d, time varying etc).

2 Element type specification (triangular, quadrilateral, tetrahedron).
3 Definition of physical properties.
4 Discretisation - creation of interconnected pieces (elements).
5 Definition of boundary conditions.
6 Formation of the element equations.
7 Formation of the system equations.
8 Solution of the equations.
9 Postprocessing to analyze the results.

In the commercially available packages, it is a common practice to execute the steps 6 to 9 in a batch form such that it is not visible to the user.

2.3.1 THE ELEMENT AND ELEMENT TYPES

The element is the critical part of the FEM. The element interconnects degrees of freedom, establishes how they act together, and determines how they respond to applied actions. Every element has one or more nodes that lie along its boundary. Nodes are the points where other elements can be connected and also at which the degrees of freedom are located. Information is passed from element to element only at common (shared) nodes. The number of degrees of freedom (DOF) at a node and their meaning (for example displacement or temperature) are determined by the element type.

The type of element used depends upon the problem. The element [K] matrix relates the applied action to the degrees of freedom in the element. In order to determine the [K] matrix, element shape functions must be determined for each type of element. An element shape function maps values of a degree of freedom from the nodes to points with in the element. This is important because the FEM solves for degree of freedom values only at the nodes. For example consider a four-node 2-D solid element for

which the values of the degrees of freedom at its four nodes have been established. Furthermore consider a quadratic distribution of degree of freedom values shown against the edge of an element Figure 2.1a. A single element with a linear shape function would do a poor job of capturing the actual quadratic nature of the response Figure 2.1b. Better results could be obtained with a greater number of elements Figure 2.1c. A single element that has a quadratic shape function can capture the actual distribution Figure 2.1d. Note that in each of these examples, the DOF were actually matched at the nodes, but not always within the elements.

Additional solution data, such as structural stress and thermal gradients, are usually derived from the DOF solutions by calculating derivatives of the shape function. Therefore, if the DOF solution captured by the shape function within the element is inaccurate, the derived results will also be inaccurate. Once the shape function have been assumed, the [K] matrix can be derived see the FE theory section.

2.3.2 THE ELEMENT MESH DENSITY

In the early development of the finite element method the programmers were using simple elements, having linear approximation functions. Employing such elements necessitates using a finely divided mesh if results were to be accurate. Since, generally, as the number of elements is increased in a mesh the accuracy of the solution is also increased. This is clearly demonstrated by Lewis [41] who compared graphically the accuracy of such a system using two different element types and densities, Figure 2.2. At present, programmers can use element that offer high

accuracy therefore reducing the number of elements. Such elements employ higher order quadratic or cubic approximation functions which normally have mid-side nodes.

2.4 FINITE ELEMENT THEORY

2.4.1 ELEMENT EQUATIONS

Often (but not always) polynomials are used for the approximation functions. They are easy to formulate, differentiate or integrate and the results may be improved by increasing the order of the polynomial. The degree of the polynomial chosen depends on the type of element. The dependent field variable, u(), in a linear three dimensional element may be represented by the form

$$u(x,y,z) = c_0 + c_1x + c_2y + c_3z \qquad (2.1)$$

where c_0 to c_4 are constants and x, y and z are independent variables, usually coordinates.

(a) 1-D Quadratic

$$u(x) = c_0 + c_1x + c_2c^2 \qquad (2.2)$$

(b) 1-D Cubic

$$u(x) = c_0 + c_1x + c_2x^2 + c_3x^3 \qquad (2.3)$$

Elements may be classified according to the order of the polynomial used to represent

the field variable within the element. Although the simplest general form of polynomial approximation is

$$u(x) = c_0 + c_1 x + c_2 x^2 + \ldots\ldots + c_{M-1} x^{M-1} \tag{2.4}$$

However, when written in this form the value of a coefficient (other than c_0) has no direct relationship to the value of u(x) at a particular point. An alternative form is:-

$$u(x) = u_1 N_1(x) + u_2 N_2(x) + \ldots + u_M N_M(x) = u_i N_i(x) \tag{2.5}$$

The functions N_i are called shape functions or trial functions as they are functions of geometry. The u_i are the unknowns, often called the degrees of freedom (DOF). In this expression the coefficients u_i are the values of u(x) at a set of M point x_i, while functions $N_i(x)$ are polynomials of degree M-1 possessing the property $N_i(x_j) = \delta_{ij}$. Therefore, $N_i(x_j)$ is 1 if i=j and 0 if i is not equal to j. Equation (2.5) in which a function u(x) is represented as linear combination of M independent functions $N_i(x)$, is analogous to the equation $u = u_i n_i$, in which a vector u is represented as a linear combination of M independent unit vectors n_i, u and n_i being vectors in a Euclidean space of P dimensions (P is greater or equal to M).

Equation (2.5) is useful for the computer approximations to more complicated known functions. If a given function f(x) has values $f(x_j)$ at a set of M arbitrary points x_j, the approximation $u(x) = f(x_i)N_i(x)$ is equal to f(x) whenever $x = x_j$, by virtue of the definition of the function N_i.

2.4.2 ASSUMED DISPLACEMENT FUNCTION USING GLOBAL COORDINATE SYSTEM

Simplex elements are elements with either linear or constant interpolation polynomials. Line, triangle and tetrahedron are the simplex elements in one, two and three dimensional cases respectively. For a one-dimensional case the linear displacement function (straight line) is a first-order polynomial which can be represented in the form

$$u(x) = c_1 + c_2 x \tag{2.6}$$

Next, if C_i the coefficients is converted into quantities that have physical meaning. This function must pass through the values of u(x) at the end points of the element at x_1 and x_2. Therefore, substituting the nodal displacements and the coordinates into (2.6), we have

$$u_1 = c_1 + c_2 x_1$$

$$u_2 = c_1 + c_2 x_2$$

where $u_1 = u(x_1)$ and $u_2 = u(x_2)$. Now, solving for the coefficients C_1 and C_2 :

$$c_1 = \frac{(u_1 x_2 + u_2 x_1)}{(x_2 - x_1)} \tag{2.7}$$

$$c_2 = \frac{(u_2 - u_1)}{(x_2 - x_1)} \tag{2.8}$$

where $L = x_2 - x_1$.

Substituting these results into equation (2.6) gives us

$$U = N_1(x)u_1 + N_2(x)u_2 \tag{2.9}$$

$$\textit{where} \quad N_1(x) = \frac{(x_2 - x)}{L}$$

$$\textit{and} \quad N_2(x) = \frac{(x - x_1)}{L}$$

$$\textit{and} \quad L = (x_2 - x_1)$$

Equation (2.9) is a function defining the displacement of any point in the element in terms of the nodal displacements(u_1 and u_2). Therefore, it can be employed to calculate intermediate values between them. The sum of the interpolation functions is always equal to one. They also hold the value of 1 at the nodes to which they apply and zero at all other nodes.

$$\textit{e.g. when} \quad x = x_1 \quad N_1(x) = \frac{(x_2 - x_1)}{L} = 1$$

$$when \quad x = x_2 \qquad N_1(x) = 0$$

2.4.3 PROPERTIES OF ELEMENTS

After the discretisation of the continuum and selection of the their interpolation functions, the matrix equations can determine by expressing the properties of the individual elements. For this, one of the four approaches of a) direct approach, b) variational approach, c) weighted residual approach, or d) energy balance approach can be used. The approach used depends entirely on the nature of the problem.
The first approach to obtain the element properties is called the 'direct approach' because its origin is traceable to the direct stiffness method of structural analysis. The direct approach can be used only for relatively simple problems.

Element properties obtained by the direct approach can also be determined by the more versatile and more advanced 'variational approach'. The variational method involves the integral of a function that produces a numerical value. When the function produces a minimum it approximately satisfies the specific differential equation that the function represents. For problems in solid mechanics, this function may turn out to be the potential energy or the complementary potential energy.

The third and even more versatile approach to obtain element properties is known as the 'weighted residuals approach'. Weighted residual methods also involve an integral. In these methods, an approximate solution is substituted into the differential equation. Since the approximate solution does not satisfy the equation, a residual or error term

results. The weighted residual methods require that the residual R(x) is multiplied by the weighting function $N_i(x)$, and the integral product of the product is required to be zero. The number of weighting functions equals the number of unknown coefficients of the approximate solution. These methods can usually be defined as collocation methods, subdomain methods, least square methods or Galerkin's method. Since the weighted residual approach does not rely on a functional or a variational statement it becomes possible to extend the finite element method to problems where no functional is available or exists.

A fourth approach relies on the balance of thermal and/or mechanical energy of a system. The 'energy balance approach' requires no variational statement and hence expands the range of possible applications of the finite element method [42].

2.4.4 ELEMENT EQUATIONS ASSEMBLY

The properties of the overall system can be constructed by "assembling" all the element properties or combining the matrix equations expressing the behaviour of the entire solution region or system.

The overall equilibrium equation can be formulated as follows for a problem in elasticity:

$$[k]\ u' = p'$$

where [k] is the assembled stiffness matrix

u' is the vector of nodal displacements

p' is the vector of nodal forces for the entire system

The assembly procedure is based on the continuity principal that, at a node where elements are connected, the values of the field variable is the same for each element sharing that node. The assembly process gives a set of linear simultaneous equations that must next be modified to incorporate the boundary conditions and constraints of the problem and thereafter can be solved in order to obtain the unknown nodal values of the field variable.

2.4.5 SOLVING THE SYSTEM EQUATIONS

For linear problems, the equations can be solved by using a number of standard techniques [43]. But for non-linear problems the solution must be obtained iteratively, each step involving the modification of the stiffness matrix [k] and/or the load vector p'. Non-linearities arise, for example, when material properties are function of temperature.

Finally, it may be required to use the solution of the system equations to calculate other important parameters such as strains and stresses from displacements or heat flows from temperatures.

PART II THE FINITE ELEMENT PACKAGE ANSYS

2.5 FINITE-ELEMENT PACKAGES RELEVANT BACKGROUND

Throughout 1970s, pre- and post-processors of commercial finite element programs evolved to simplify the data preparation and manipulation of results. One of the important tasks performed by the former is mesh generation. Early programmes used simple mesh generation routines and had limited graphical display capabilities. Postprocessors have been developed to enhance the interpretation, reorganization and reduction of the solution output. A decade later, the concept of general purpose mesh generators came about. These programs were different from the previous programs in that they executed interactively.

2.6 INTRODUCTION TO ANSYS

ANSYS is a self-contained general purpose finite element program developed and maintained by Swanson Analysis Systems Inc. The program contains many routines, all inter-related, together they provide solutions to modern engineering problems by finite element method.

ANSYS may be executed in either of two modes: 1) interactive, or 2) batch. An analysis execution may be "all batch", "all interactive", or a combination of both. The element library provides more than forty element types, for static and dynamic analyses, and twenty for heat transfer analyses. This variety of elements gives the ANSYS program the capability of analyzing many two- and three- dimensional

engineering problems. Loading on the structures may be force, displacements, pressures, temperatures or response spectra. For the heat transfer, the loading may be heat flows, specified temperatures, internal heat generation, radiation or convection at the component surfaces.

An engineering problem is usually solved in three phases: preprocessing, solution and postprocessing Figure 2.3. ANSYS has two preprocessing routines available, known as PREP7 and PREP6. The former contains a powerful mesh generation capability and is able to define all other analysis data such as real constants, material properties, constraints, boundary conditions and loads, where as the latter generates load step for multiple load step type analysis such as transient problems.

After completion of preprocessing, the solution phase may begin. The solution phase involves operation on the model data to produce solutions for the unknowns at the nodes in the model. The solution phase may consist of several solutions in series, such as a thermal solution, followed by stress solution. This solution phase of the ANSYS is executed in a batch form and is not seen by the user.

Upon the completion of the solution phase, postprocessing may begin. This provides interrogation of the results from the solution phase. The ANSYS program has several routines for postprocessing analysis results such as POST1 and POST26. POST1 is a General Database Results Postprocessor, whilst POST26 is a Time-History Results Postprocessor.

2.6.1 ISOPARAMETRIC THERMAL SOLID - STIF, 70

This element has a three-dimensional thermal conduction capability. The element has eight nodal points with a single degree of freedom, temperature, per node. The geometry, nodal locations, face numbers, loading, and the coordinate system for this element are shown in Figure 2.4. The element is applicable to three-dimensional, steady-state or transient, thermal analyses. The element is defined by eight nodal points and the material properties: thermal conductivity, specific heat and density.

The post processing data includes those expressed per element, for example heat flux, element volume, average temperature and those per face, for example area and heat flux. A surface with no boundary condition is assumed adiabatic. Heat flowing out of the system is assumed positive.

2.7 MODEL GENERATION IN ANSYS

In ANSYS, mesh generation may be performed by either: a) direct generation or, b) automatic generation. In direct generation, the designer makes use of standard ANSYS commands, such as N, FILL and NGEN to generate nodes and E and EGEN to generate elements. Automatic mesh generation in ANSYS uses solid modelling concepts to mesh portions of a model. A region once generated may be modified, or partially regenerated. The automatic mesh generation procedure may be used in conjunction with the direct generation procedure.

During the model generation, in particular direct generation, the designer may be forced to generate an element of poor quality such as one with large twisting. In this case, triangular elements may offer a better solution. Triangular elements may also be employed for modelling transition regions between fine and coarse grids or for modelling irregular structures. Nevertheless, the best shaped elements in two and three dimensional analyses are quadrilateral and brick elements.

2.7.1 PARAMETRIC APPROACH IN ANSYS

After the mesh generation and submission of the model to the solution phase, the calculated results may be extracted and analyzed. In some cases, the analysis of the data may indicate that part or whole of the model is not of sufficient accuracy and therefore it should be modified and re-meshed. In other cases, the designer may need to generate several models of similar geometry. In such cases, the global control features of the ANSYS program may be used to control the model generation based on specified variables and/or selected analysis criteria. The global controls may be used to control many aspects of the model such as mesh refinement and interrogate of the obtained results. To this end, these controls gives the designer the capability to run an analysis virtually automated. These features are known as parameters and repeat routines. The latter consist of macros, branching and user files.

This feature was used in this investigation to conveniently perform calculations and/or define the boundary conditions such as heat transfer coefficient and physical properties

2.7.2 BOUNDARY CONDITIONS FOR ELECTRONIC SYSTEM ANALYSIS

In a thermal analysis the following heat transfer mechanisms may be present:

(1) convection,
(2) conduction,
(3) radiation
(4) contact resistance.

The heat transfer coefficients in an electronic system may be predicted by incorporating available correlations in to a FE program. Alternatively the FEM may be used in conjunction with experimental measurements to predict such correlations.

The load conditions can be varied by varying the properties of the elements, the internal heat generation or cooling conditions.

2.8 CONCLUSIONS

This section has briefly described some basic finite element concepts, and introduced the ANSYS FE package used in this research. A summary of these concepts are as follows:

1) The finite element method approximates engineering problems by using discrete, interconnected elements.

2) The use of finite elements rather than a rectangular grid (as in finite difference) provides a much better approximation for irregularly shaped systems.

3) The finite element method has two important features that distinguish it from other numerical methods:

a) a complex problem can be reduced to the consideration of a number of greatly simplified problems

b) The properties and characteristics of individual elements are capable of wide variation, each suitable to different applications.

4) Degrees of freedom are located at the nodes of each element and represent the unknown response to applied action.

5) Each element also has an assumed shape function which acts to map degree of freedom values from the nodes to points within the element. This is then used to form an element [K] matrix that establishes the relationship between the degree of freedom and the applied actions for that element.

6) There are four different approaches in formulation of element properties

a) direct approach

b) variational approach

c) weighted residuals approach

d) energy balance approach.

7) The execution of the finite element method follows a standard step-by-step procedure starting from the model abstraction to postprocessing of the results.

8) The finite element method may be used for the analysis of electronic components, replacing the traditional trial and error methods.

9) By using FEM, design parameters such as temperature distribution and stress levels in an electronic system can be predicted with accuracy for models which are a realistic representation of the real design system.

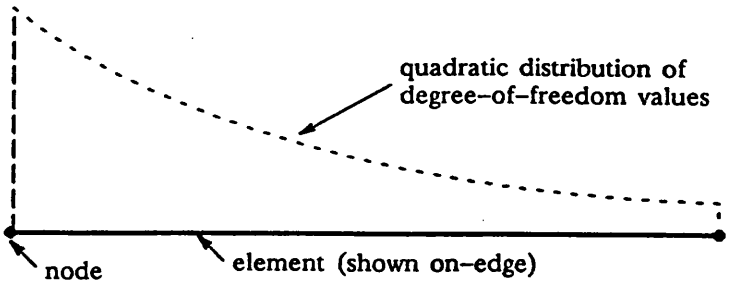


FIGURE 2.1a - ASSUMED QUADRATIC FUNCTION

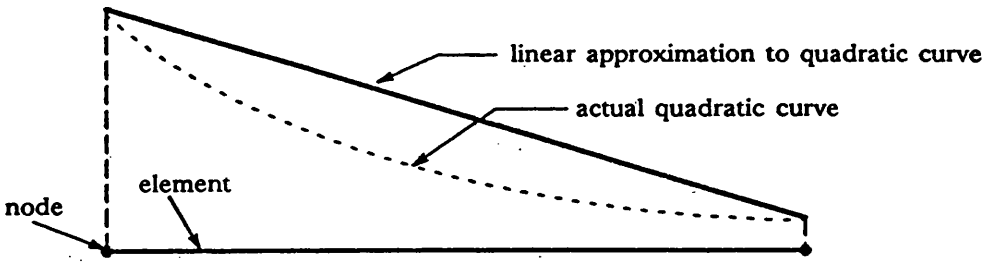


FIGURE 2.1b - LINEAR APPROXIMATION

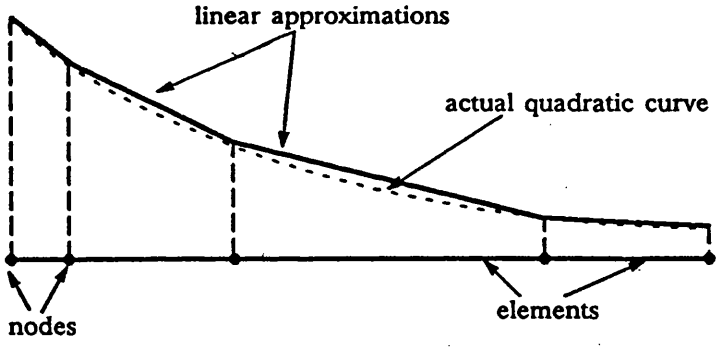


FIGURE 2.1c - SEVERAL LINEAR APPROXIMATION

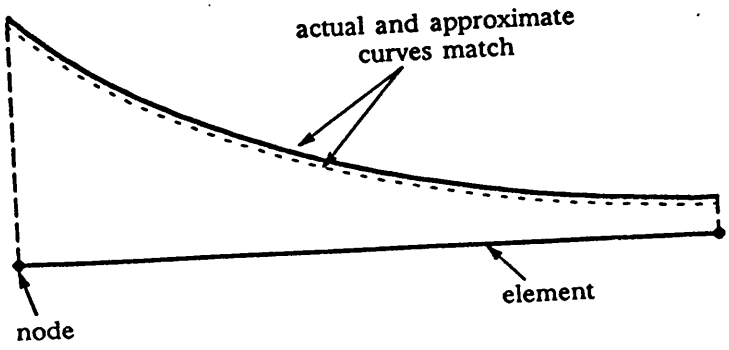


FIGURE 2.1d - ACTUAL SHAPE FUNCTION

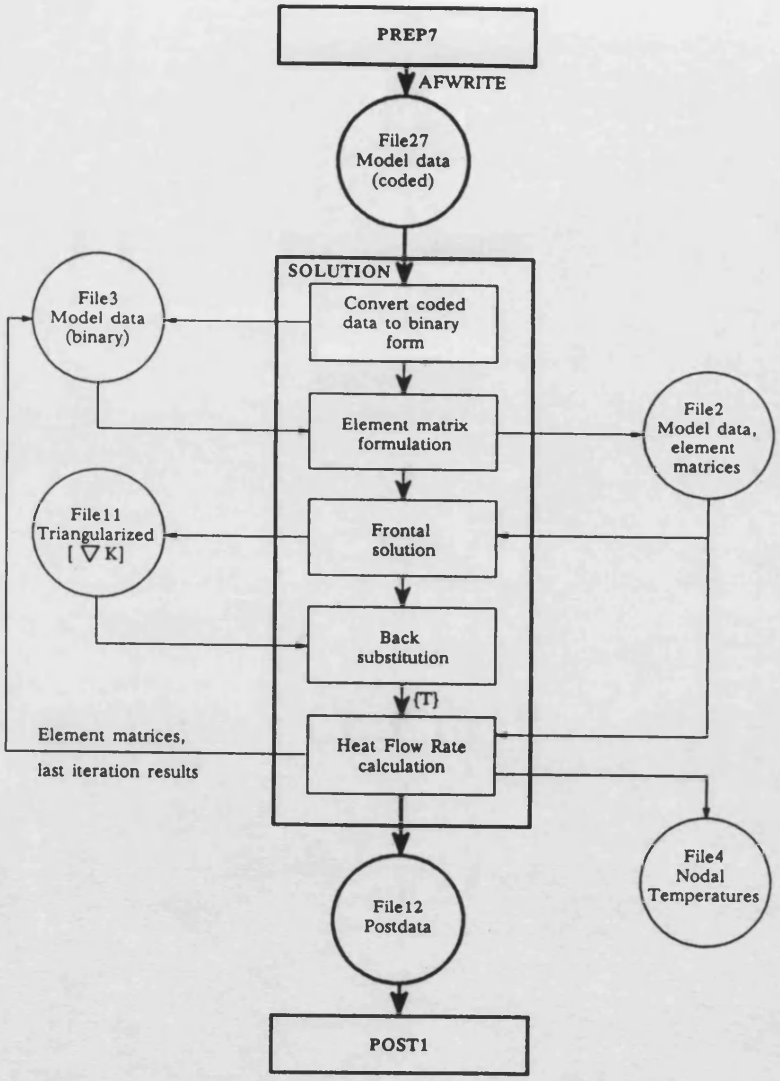


FIGURE 2.3a - STEADY-STATE ANALYSIS DATA FLOW

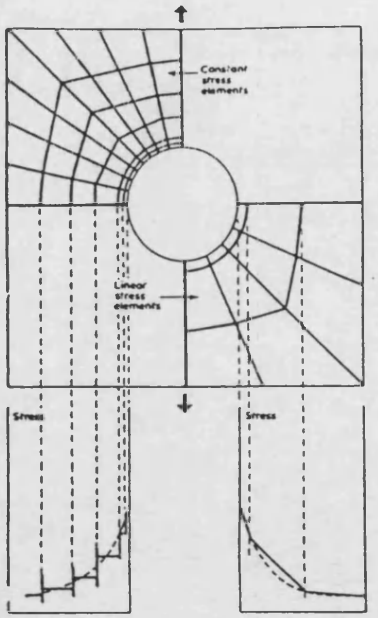


FIGURE 2.2 - STRESS AROUND A HOLE IN A PLATE UNDER UNIAXIAL TENSION

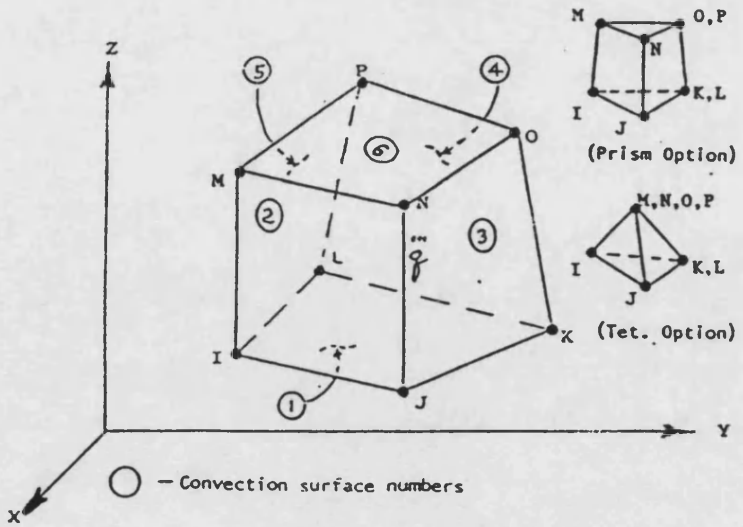
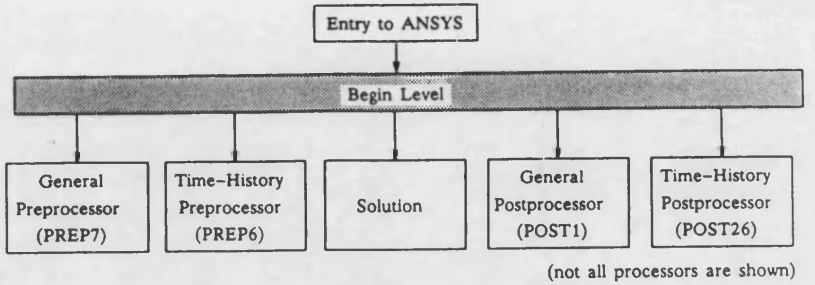


FIGURE 2.4 - ISOPARAMETRIC THERMAL SOLID (STIF, 70)



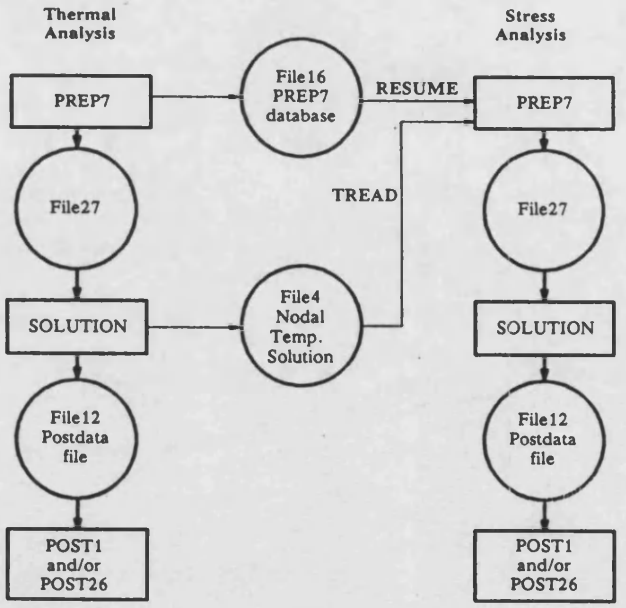


FIGURE 2.3b - THERMAL-STRESS ANALYSIS PROCEDURE

CHAPTER 3

A TEST RIG FOR EXPERIMENTAL HEAT TRANSFER RESEARCH INTO COOLING OF MICROELECTRONIC COMPONENTS (PACKAGES) MOUNTED ON PCB

3.1 INTRODUCTION

Air is widely used as a cooling medium because of its long established technology, simplicity and low cost. Unfortunately, there appears to be lack of precise, well documented heat transfer data appropriate to the particular geometries used in electronic applications.

Accurate thermal test measurements are difficult on PCB/Package systems with conventional measuring techniques for two principal reasons:-

a) The chip itself, the source of heat, is extremely small (typically 2mm square). It is not directly accessible being encapsulated within the package.

b) Although air flow over the surface of the PCB may be generally characterised as being a boundary layer, in fact the flow regime is more complex. Because of their relatively large size, the packages form obstacles which interrupt the flow.

The test rig was designed to provide reliable data from which steady-state heat transfer correlations could be deduced.

Although theories are available in the literature which evaluate boundary layer development on a flat plate, theoretical analysis of forced convection cooling of

discrete modules mounted in a substrate is beyond the state of the art, even for the two-dimensional idealization. However, a thermal map of sufficient accuracy can, in principle, be obtained by use of numerical techniques (FE). Such techniques often require specification of the heat transfer coefficient. This parameter is, however, strongly influenced by the physical and thermal boundary conditions, as well as by the flow regime and state of boundary layer development. Consequently, use of a Nusselt number obtained from fully developed correlations and/or analysis may lead to grossly erroneous results, and care must be taken to base the analytical or numerical calculation on value, or values of the heat transfer coefficient appropriate to the thermo-fluid classification.

3.1.1 RELEVANT PREVIOUS WORK DUCT FLOW

The heat transfer coefficients associated with axially invariant but different heat fluxes have been studied in detail by Lundberg et al [44]. As part of a comprehensive examination of asymmetric heating in annuli, the results of this study were presented in terms of the Nusselt number, which corresponds to parallel plate channel and can be applied to the electronic PCBs stacked in a cabinet. Sparrow et al [45] investigated the heat transfer and pressure drop characteristics of array of heat generating rectangular modules that are commonly encountered in electronic equipment. Baraaten and Patankar [46] studied the heat transfer characteristics through shrouded arrays of rectangular blocks simulating the electronic packages. However their studies were limited to fully developed laminar flow. Flow visualisation between two parallel plates with aid of rectangular turbulence promoters was investigated by Kang et al [47].

3.1.2 AIR JET IMPINGEMENT

The application of high velocity air jets to heat or cool a normal heat transfer surface has tremendous engineering potential. However, due to the complexity of the system, no firm theoretical treatment has yet been evident and only very scant experimental data are available in literature. Vickers [48] studied local heat transfer coefficients of fluid jet impinging on a plane surface with laminar flow. His empirical equations applied to Reynolds number in the range 250 to 950. The distance between the jet orifice and the surface of the target plate ranging from 8D to 20D, and the values of X/D = 1 to 3.2 (diameter of the orifice being held at D = 0.0507 in). Gordon [49] measured local, as well as average heat transfer coefficients for single and multiple nozzle jets at a Reynolds number of 7000 to 112,000 with the nozzle diameter 0.125 to 0.354 in. Freidman and Mueller [50] reported their experimental data recording average heat transfer rates of multiple jet air flow from slots, holes and nozzles parallel to, or impinging on, the heat transfer surface. They studied the effects of injection angle, spacing, hole size, free open area of jets, and plate width, on heat transfer coefficients. Perry [51] made further studies on the effect of impingement angles. The maximum gas temperature and velocity being 750 deg F and 250 ft/sec. Daane and Han [52] investigated the interference of the impingement air flow with the spent air exhaust flow in multiple jet systems.

3.2 HEAT TRANSFER BACKGROUND

Engineering thermal analysis of electronic systems is based on any or all of three methods of thermal-energy transport: conduction, convection and radiation.

For better understanding it is convenient to characterise the modes of heat transfer in an electronic package as follows:

i) Internal conduction within the body of the package.

ii) Convection from the outside surface of the package (case).

iii) Radiation transfer between the packages.

iv) Cumulative bulk temperature rise of the coolant in its passage through the enclosure which houses the PCBs.

i) ***Conduction***

Fourier's Law of conduction in a solid or a stationary fluid is frequently used in its 1-dimensional steady-state form:

$$Q = -k A \left(\frac{dT}{dx} \right) \qquad (3.1)$$

where:-

Q = Heat transfer rate, W
A = Cross-sectional area of heat flow path, m^2
dT/dX = Temperature gradient, ° C/m
k = Thermal conductivity, W/° C

The thermal conductivity is a physical property which is dependent on the specific material involved. While it is not uncommon for k to be temperature dependent, the error in assuming a constant value is usually acceptably small. Fourier's Law is analogous to Ohm's law. Thus equation 3.1 may be expressed in terms of the thermal

resistance R of the package and then directly integrated. Rearranging the variables:

$$dT = -\left(\frac{Q}{kA}\right) dx \tag{3.2}$$

$$\int_{T1}^{T2} dT = -Q \int_{x_1}^{x_2} \frac{dx}{(k\,A)} \tag{3.3}$$

If A and K do not vary over the path length $L = x_2 - x_1$

$$\Delta T = \left(\frac{L}{k\,A}\right) Q \tag{3.4}$$

where; $\Delta T = T_1 - T_2$ the temperature difference over L. The quantity preceding Q is a thermal resistance for conduction;

$$R = \int_0^L \frac{dx}{(k\,A)} \tag{3.5}$$

Generalisation of Fourier's Law to three dimensions is accomplished by carrying out a steady-state energy balance on an element of volume $\Delta V = \Delta x\ \Delta y\ \Delta z$ as shown Figure 3.1a.

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) = -Q_V \tag{3.6}$$

Not all practical problems are steady state. The temperature/time relationship of a

package may be of interest during the heating up phase. The steady state energy balance must be modified to account for the change in the energy stored within the control volume.

$$\rho \, \Delta V \, C_p(\frac{\partial T}{\partial t}) \tag{3.7}$$

This yields the general time-dependent conduction equation:-

$$\frac{\partial}{\partial x}(k_x \frac{\partial T}{\partial x}) + \frac{\partial}{\partial y}(k_y \frac{\partial T}{\partial y}) + \frac{\partial}{\partial z}(k_z \frac{\partial T}{\partial z}) = -Q_V + \rho \, C_P \, (\frac{\partial T}{\partial t}) \tag{3.8}$$

ii) ***Convection***

Convection from the external surface of the package varies with location, therefore, the rate equation in differential form can then be written as:-

$$dQ = -h \, dA \, (T_f - T_s) \tag{3.9}$$

where:-

h = Surface heat transfer coefficient, W/m^2 K
A = Area of convective surface, m^2
T_s = External surface temperature, • C
T_f = Temperature of the fluid, • C

The convective thermal resistance can be written as:-

$$R = \frac{1}{h A} \tag{3.10}$$

Low values of h would generally be associated with natural convection in a gas, high values with forced convection and liquid cooling. In forced convection, h is principally

dependent on the properties of the fluid and its velocity; as such its value can be controlled independently. In contrast, in natural convection, h is a function of buoyancy forced which depend upon temperature differences between surface and fluid which are not under independent control.

iii) ***Radiation***

Finally, there will be an exchange of radiation between the surface of the package above absolute zero and its surroundings. This may be evaluated by the Stefan-Boltzmann Law:-

$$Q = \sigma \epsilon A (T_C^4 - T_A^4) \qquad (3.11)$$

where:-

σ = Stefan-Boltzmann constant, $W/m^2 K^4$
ε = Emissivity
T = Absolute temperature, K

When a package is surrounded by other packages at roughly the same temperature, the net radiation exchange will approach zero, and is usually neglected. However when the convection coefficients are low, and the surroundings are cold, radiation should not be ignored.

3.2.1 NUSSELT NUMBER AND PRANDTL NUMBERS

Heat transfer across a solid (package surface) to air interface is illustrated in Figure 3.1b. A thin thermal boundary layer exists such that very close to the wall surface the dominant heat transfer mechanism in the air is molecular conduction. The fluid heat transfer to the surface may be expressed in terms of both equations 3.1 and 3.9;

$$dQ = -K\,dA\,\left(\frac{dT}{dX}\right) \tag{3.12}$$

$$dQ = h\,dA\,(T_s - T_f) \tag{3.13}$$

Then Nusselt number (Nu) can be expressed as;

$$Nu = \frac{h\,x}{K} \tag{3.14}$$

The Nusselt number may be regarded as a dimensionless heat transfer coefficient.

The Prandtl number (Pr) can be expressed as;

$$Pr = \frac{momentum\ diffusivity}{thermal\ diffusivity} = \frac{\nu}{\alpha} = \frac{\mu\,C_p}{K} \tag{3.15}$$

where:-

μ = Absolute viscosity, kg/m s
C_p = Specific heat at constant pressure, J/kg K
K = Thermal conductivity of air, W/m K

Prandtl number relates thermal boundary layer to momentum boundary layer.

where:-

$$\alpha = \frac{K}{\rho\,C_p} \quad THERMAL\ DIFFUSIVITY$$

$$\nu = \frac{\mu}{\rho} \quad MOMENTUM\ DIFFUSIVITY$$

3.2.2 FREE AND FORCED CONVECTION

Free convection occurs when a solid and the surrounding air are at different temperatures. Heat flowing to or from the fluid produces differences in density and buoyancy forces, which in turn cause air displacements (convection currents).

A dimensionless quantity unique to free convection is the Grashof number (Gr), the ratio of buoyancy to viscous force:

$$Gr = \frac{g\,\rho^2}{\mu^2}\,\beta\,(T_s - T_f)\,x^3 \qquad (3.16)$$

where:-

g = Acceleration due to gravity, m/s^2
β = Coefficient of cubical expansion for a perfect gas, 1/K
T_s = Surface temperature, $^\bullet C$
T_f = Ambient fluid temperature, $^\bullet C$
x = A characteristic dimension

Free convection heat transfer data are usually expressed in the form of a non-dimensional correlation:-

$$Nu = C\,(Gr\,Pr)^n \qquad (3.17)$$

In the case of forced convection heat transfer buoyancy forces are considered negligible, and the Reynolds number (Re) is used to characterise the dynamic state of the fluid :-

$$Nu = C\,(Re)^m\,(Pr)^n \qquad (3.18)$$

Provided that heat transfer correlations such as the above are available for a particular

geometric configuration they can be used to determine the heat transfer coefficient along a surface. However, they were not available for electronic components, and it was an important objective of this research to carry out experimental and theoretical investigations to establish them.

3.3 OBJECTIVES

The main objectives of this part of the research are as follows;

i) To assess the suitability of the test rig for carrying out heat transfer measurements on an instrumented PCB, and to modify it as necessary.

ii) To investigate the thermal and fluid boundary layer, and obtain typical temperature distribution of the components on the PCB under uniform heating condition at varying velocities and power configurations. These temperature distributions would then be used to deduce dimensionless heat transfer correlation for the configuration tested.

3.4 APPARATUS AND GENERAL DESCRIPTION OF THE TEST RIG

The general arrangement of the research rig, in its original configuration is illustrated in Figure 3.1c. Ambient air from the laboratory was discharged at the outlet through the test section by a variable inlet fan driven by a 3-phase electric motor. The cooling air was then directed to the working section by means of 24 mm steel piping and a diverging diffuser. The working section of the rig includes test section, dummy section and component free exit length. The test duct is constructed of perspex sheets (10 mm thick) in order to reduce the heat loss through its walls. The dummy section consists of a honeycomb flow straightener and an array of plastic moulded PCBs. This section

is included in order to provide well defined, reproducible fully developed flow into the leading edge of the test section. The exit length is to provide flow pattern repeatability for the last row of components on the PCB. The test section houses an instrumented PCB mounted between two other similar PCBs which act as flow guides. Thermocouple leads from the PCB under investigation are passed through the side wall via standard euro-connectors. The total air flow in the rig is measured by means of a British standard orifice plate.

3.5 INSTRUMENTED PRINTED CIRCUIT BOARD ASSEMBLY

Although with small adjustments the test facility can accommodate a variety of PCB/package combinations, this description is related to the particular combination installed for the present investigation.

The PCB is a multilayer double Euro-Card, on which is mounted a rectangular array of 16-pin dual-in-line package (DIP), ceramic wirewound resistor packs (Beckman 898-3-R680), see Figure 3.2. It should be noted that although the external appearance of these packages are similar to that of a real logic DIP, their internal structure is somewhat different. Each resistor pack consists of a central layer of eight separate 680 ohm resistances connected in parallel to form an effective resistance of 85 ohm/pack. This central layer is encapsulated between two blocks of ceramic to form a solid block, with two rows of leads on either side soldered into the PCB. These devices offer the operational advantage that the power dissipated within them can easily be controlled and measured, by varying the voltage level across the supply leads.

However, it should be remembered that the power dissipation is distributed over the entire central layer, rather than being restricted to the small volume of the chip in a real logic DIP. The temperature of each package is measured by means of a miniature bead thermistor glued to the centre of the under surface Figure 3.2.

The PCB which measures 160mm x 233mm x 1.6mm is of composite construction and is fabricated by gluing together two double-sided G10 fibreglass cards. The resultant 7 layer board is illustrated in Figure 3.3. Tracks which transmit the power supply and the thermistor signals, to and from individual packs are incorporated in the 4 copper layers, also shown in Figure 3.3. The board is connected to the external system by means of Standard Euro edge connectors and cables.

3.6 AIR-FLOW MEASUREMENTS

The total mass flow rate of the system is measured from the pressure drop across a calibrated British Standard orifice plate (BS 1042) with D and D/2 pressure tapping Figure 3.4. The volume flow rate Q (m^3/s) can be determined from the following expression (obtained by substituting the appropriate numerical values into the basic equation in BS 1042)

$$Q = 0.0028352 \sqrt{\Delta h} \qquad (3.19)$$

The flow rate evaluated from equation 3.19 was checked by pitot-tube measurements, using two methods.

In the first (Figure 3.4b), the pitot tube registered the air velocity at the centre of each of five equal areas. In the second, Figure 3.4c, the pitot tube was positioned at a distance 3/4 of the pipe radius from the centre line. At this position, the pitot will indicate the average velocity in the pipe, over quite a wide range of Reynolds number.

The pressure across the orifice plate was also verified with a sensitive pressure transducer (range ± 125mm H_2O) whose output signal is connected to the data acquisition system. There is a linear relationship between the transducer output voltage (ΔV) and the pressure difference across the orifice (Δh), so that these two variables may be related by the expression:-

$$\Delta V = 2509.52 + 24.09\ \Delta h \qquad (3.20)$$

where:-

ΔV = Transducer output voltage, mV
Δh = Orifice pressure difference, mm H_2O

The heat transfer rate in the test section must be related to the air pressure drop across it. Accordingly the static pressure at inlet to the test section is measured at five tappings, 30cm apart across the duct. When connected to a common header, these tappings register the average static pressure at inlet. A similar set of five tappings registered the average static pressure at outlet from the working section.

3.7 DATA ACQUISITION SYSTEM

3.7.1 GENERAL DESCRIPTION

The main components of the data acquisition system are as follows:-

i) Interface unit

ii) "Mowlem", Autonomous Data Acquisition system (ADU)

iii) Microcomputer

These three components are arranged as illustrated in Figure 3.5. The Mowlem ADU (a proprietary device) which is the heart of the system, is the unit nearest to the computer. The ADU is based on a microprocessor card which accesses a 16 k-byte memory card, and runs under its own operating system.

Data from the measuring instruments is collected by the ADU which is interfaced to an IBM computer via an RS 232 port. The software package [31] converts the data into the required form and displays it on the computer screen. A permanent record of all the data for a particular test can also be obtained in the form of a permanent copy. The ADU is programmed to carry out automatically a variety of data logging, control and monitoring tasks. This program also makes it possible to control the power of the electronic modules via the computer keyboard.

The program has the facility to give a graphical display of chip temperatures. It displays a 4 x 13 block array, representing the chips on the PCB. Each of the 52 chips temperature is then given a colour coding corresponding to its temperature.

3.8 MODIFICATIONS OF THE TEST RIG

The test rig was initially configured so that air from the fan outlet was discharged through the rig Figure 3.1. However, this system proved to have some disadvantages. Even with the test board powered uniformly, early tests showed non-uniform cooling of the PCB. This was diagnosed to be caused by extraneous heating and non-uniform velocities imparted to the air by the fan.

These undesired effects were eliminated by placing the fan downstream of the rig so that it operated as an induced draught system Figure 3.6. With this new configuration ambient air from the laboratory was drawn through the test section. Care was also taken to ensure uniform inlet conditions by fitting a diffuser at inlet.

3.9 METHOD OF TESTING

Precise and accurate values of heat transfer coefficient are difficult to measure in an electronic card system, because the heat flux is distributed in a complex and unknown manner over the various surfaces. In practice the air flow regime is different on either side of the PCB, hence producing different heat transfer coefficients and surface temperature. Measurement of the power conducted through the package leads to the flat under-surface of the PCB is invaluable, but is a complicated practical task to achieve. To overcome this difficulty, two different experimental procedures were adopted.

i) Before any tests could be carried out the effect of the 75mm gap immediately upstream of the test section (Figure 3.7a) on the fluid boundary layer had to be investigated. In order to eliminate the effect of thermal boundary layer, a series of tests involved powering the modules in the test board one row at a time. Each test was conducted with three different arrangement of dummy boards;

a) dummy board in place as shown in Figure 3.7a,

b) without dummy boards, and

c) dummy boards moved close to the test section to eliminate the gap.

ii) With the new configuration of the dummy boards, heat transfer from the under-surface of the test board was eliminated by placing a similar PCB in back to back contact with it. Both PCBs were powered to the same power level. High thermal conductivity paste was used between the two PCBs to overcome the contact resistance problems, and electrically insulate the exposed pins on the back of the board. With this new arrangement, any power dissipated in the system can be transferred to the cooling air only from the side of the board on which the packages are mounted. Since the power dissipated is known, convective areas defined, and temperature values recorded, then at any streamwise location the convective film coefficient for air flow over the modules can be obtained.

With this configuration, a number of experiments were carried out with variable component heat dissipation rates (0.2-0.8 W/chip) and air velocities (3 - 15 m/s). The

limits of the power and velocity chosen was to aid comparison of data with the available literature.

iii) This test was rather different. It involved the use of a jet-plate with a particular hole configuration ϕ 2mm. This caused each chip to be cooled by its own turbulent jet of cooling air Figure 3.7b. Ideally any boundary layer (thermal or fluid) that were created, would be constant over the board and thus would not give an uneven temperature distribution. In all cases, the package temperatures was related to the inlet air temperature. Hence package temperatures are expressed as "temperature above ambient".

3.10 DISCUSSION OF RESULTS

3.10.1 EFFECT OF REYNOLDS NUMBER

In general, the type of flow in a smooth duct, either laminar or turbulent is determined by the magnitude of the Reynolds number which is defined by :-

$$Re = \frac{\rho VL}{\mu} \qquad (3.21)$$

where:-

ρ = Air density, kg/m^3
V = Air velocity, m/s
L = Characteristic length (of duct), m
μ = Air viscosity, m^2/s

The important parameters governing the flow in a smooth duct are "V" and "L". The characteristic length in terms of equivalent diameter is defined as:-

$$De = \frac{4\ [duct\ cross\text{-}sectional\ area]}{wetted\ perimeter} \qquad (3.22)$$

The critical Reynolds number (Re) for a smooth duct is approximately 2000, below this the flow is laminar. Above this critical value there is a transition from laminar to turbulent flow. For most industrial applications a Reynolds number of 3000 is considered, as fully turbulent.

Typical profiles of air and component temperature over the test board are illustrated in Figure 3.8a. Taking "L" as the distance from leading edge of the board, the slope of the component temperature curve decreases up to the critical value of Reynolds number. After this critical value, the slope becomes almost constant and equal to that of the air temperature curve. Beyond the critical Reynolds number, where the fully developed thermal boundary layer exits, the heat transfer coefficient h becomes approximately constant. The heat transfer coefficient, "h" can be imagined to be an indicator of the thickness of the boundary layer, where the temperature is much higher than the mixed air temperature. Since the development of this boundary layer is at the leading edge of the PCB, the h value for the first row of packages is often twice that of the one near the trailing edge.

3.10.2 FINITE ELEMENT MODEL

The FE model used in this part of the research was the modified version of FE model presented by Hardisty et al [31] (FE model II). As illustrated in Figure 3.8b the FE

model is a fully three-dimensional detailed finite element model of a single module. The PCB is modelled in three layers of which the two outer layers consisted of epoxy fibreglass with thermal conductivity of 0.29 W/m K. The central layer is modelled as a composite of epoxy and copper with an average conductivity of 225.5 W/m K.

i) Modification of the FE model.

In the above model leads from the package were constructed to stop on the top surface of the board. This was modified so that the leads passed through the board to the under side of the PCB. In a series of tests, the FE model was used in turn to simulate the performance of each of the 13 rows on the board. This was achieved by varying the boundary conditions in the model to correspond to the local conditions of the appropriate row on the PCB.

3.10.3 THERMAL BOUNDARY LAYER INVESTIGATION

i) Dummy boards in original place.

In forced convection when the flow is enhanced between two electronic cards forming a duct, the fluid boundary layer and the thermal boundary layers are initiated due to velocity and temperature gradients respectively. The thickness of the thermal boundary layer is a major factor controlling the value of heat transfer coefficient. At the leading edge, the thin nature of this boundary layer reduces the conduction distance to the free stream and therefore, results in high heat transfer coefficient. Moving along the PCB from the leading edge, the effects of heat transfer penetrate further into the free steam and the thermal boundary layer grows. This results in a corresponding decrease in the heat transfer coefficient. If the test board is uniformly powered at a certain distance from the leading edge, thermally fully developed flow conditions are established. At

this position the local heat transfer coefficient becomes constant.

A series of tests was carried out to investigate whether or not the dummy boards were effective in producing a fully developed flow region at the leading edge of the test board. Under constant velocity and power conditions, the first row was powered while the other twelve rows remained off. The process of powering one row at a time was continued along the PCB towards the trailing edge until all thirteen rows had been powered.

The purpose of powering single rows at a time was to eliminate the effects that any nearby heated packages might cause. This meant that any difference in successive row temperatures would be due entirely to variations in the turbulent flow.
With reference to Figure 3.9, it was evident that the dummy boards separated by a 75 mm gap from the test board, has no significant effect on flow development, since similar data was obtained when the dummy boards were removed.

Figure 3.10, illustrates the effect of reducing the gap between the dummy boards and the test board to a package pitch (15 mm gap). With the new configuration, the average temperature rise of each powered row was found to be approximately the same irrespective of its location on the test board. The results of Figure 3.9 show that the effect of the 75 mm gap is to mix the flow so that the boundary layer development begins again from the leading edge of the test board. However Figure 3.10 show that when the dummy boards are close to within a single package pitch (15 mm gap), the same heat transfer coefficient is measured in each powered row. With this latter

arrangement the flow remains fully developed. This emphasises the influence of the thermal boundary layer.

3.10.4 BACK TO BACK TEST (TEST BOARD INSULATED)

The arrangement of the PCBs and the temperature distribution obtained from this test are illustrated in Figures 3.11a and 3.11b respectively. Due to elimination of the normal heat loss from the under surface of the test board modules, temperatures in these tests were high. Typical tests at power levels of 0.5 and 0.7 W/chip with velocities ranging from 3 to 10 m/s are illustrated in Figures 3.12 and 3.13 respectively. The test board is arranged in an array of 13 rows and 4 columns of packages. The temperature distribution obtained above, is the average temperature of the four packages forming a row.

Having eliminated the heat transfer from the under surface of the board, the heat transfer coefficient from the package surface to the air at any streamwise location, was evaluated using the Newton rate equation (3.9) with the measured convective surface area, monitored temperature and power input. The characteristic length and the convective surface area was based on the package surface area and the associated rectangular area of the board. This extends to a line midway between each package. At test conditions heat transfer by radiation generally was relatively small. However, for some tests at low values of heat transfer coefficient the total power measured was corrected for radiation losses by equation 3.11.

Assuming complete mixing of the air at any location x in the duct, the cumulative temperature rise of the airstream was calculated from an energy balance equation. A series of tests using the energy balance equation, and comparison with experimental measurements, for varying power and velocity is illustrated in Table 3.1. This verifies the bases of this assumption.

$$\Delta T_x = \frac{(Q_t - Q_r)}{m\, c_p} \tag{3.23}$$

where:-

ΔT = Air temperature rise, ° C
m = Air mass flow rate, kg/s
Q_t = Total power dissipation, W
Q_r = Estimated heat transfer by radiation, W

c_p = Air specific heat capacity, J/kgK

The heat transfer coefficient at any streamwise distance x was evaluated by the following equation;

$$h_x = \frac{(Q_t - Q_r)}{A\,(T_M - T_A)} \tag{3.24}$$

where:-

h_x = Heat transfer coefficient at any location x from the leading edge of the test board, W/m^2 C
A = Convective surface area, m^2
T_M = Measured temperature, ° C
T_A = Mixed air temperature at any location x, ° C

Figure 3.14a illustrates the heat transfer coefficient calculated for a typical velocity and power configuration used during the test. This figure shows that, high h values were obtained at the leading edge compared to the trailing edge of the board.

The procedure used above to predict the heat transfer coefficient at any streamwise location suffered from a limitation arising from the positioning of the transistor between the modules, Figure 3.2. As a consequence it produced h values which were lower than the expected values of heat transfer coefficient Figure 3.14b. A further shortcoming of this method, is due to the multilayer PCB, where the seven layers of copper tracks in the board act to conduct the heat from the hotter trailing edge to the cooler leading edge.

Figure 3.15a illustrates the comparison of the calculated values of the heat transfer coefficient at any streamwise location, to those predicted by Wills correlation [30], which has the form :-

$$h = 4.2 + 6.1 \left(\frac{V^{0.8}}{X^{0.3}}\right) \qquad (3.25)$$

where :-

V = Air velocity in the test section, m/s
X = The measured distance from the leading edge of the PCB, m

The percentage difference in values calculated is due to the layout of the packages on the PCB. Wills [30] work is based on the length of the components being along the direction of the flow, whereas in this research work the flow was perpendicular to the package width. This would cause an increase in turbulence which in turn will result in higher values of heat transfer coefficient, compared to those that are predicted by Wills [30] correlation.

3.10.5 A CORRELATION FORMULA FOR COMPONENT WIDTH PERPENDICULAR TO DIRECTION OF THE FLOW

Within the preceding section, a number of simplifying assumptions were made in order to predict approximate values of heat transfer coefficients. In this section, an attempt is made to build a correlation formula which will predict the heat transfer coefficients on a PCB, with the packages mounted with their longitudinal axis perpendicular to the direction of the flow (reference temperature, T_{bulk}).

The correlation formula of equation 3.25 was sought in the form:

$$h_c = C_1 + C_2 \left(\frac{V^{0.8}}{X^m}\right) \qquad (3.26)$$

where:-

C_1 = Constant of correlation for natural convection and radiation.
C_2 = Constant of correlation for turbulent flow.
V = Air velocity in the duct.
X = The measured distance from the leading edge of the PCB.
m = The index of the distance or gradient of heat transfer coefficient curve.

For a vertical plate [53]:-

$$h_c = 1.373 \left(\frac{\Delta T}{\sqrt{L \times W}}\right)^{0.25} \qquad (3.27)$$

For a horizontal plate [53]:-

$$h_c = 1.475 \left(\frac{\Delta T}{L}\right)^{0.25} \quad (3.28)$$

Evaluating C_1 (the constant of correlation for natural convection and radiation):-

For a horizontal plate;

Package width 6mm: $h_c = 5.290\ (\Delta T)^{0.25}$

Package length 22mm long $h_c = 3.830\ (\Delta T)^{0.25}$

Package length 50mm long $h_c = 2.120\ (\Delta T)^{0.25}$

This yields an average of:- $h_c = 4.043\ (\Delta T)^{0.25}$

If it is assumed that the results of natural convection,

ΔT = 1 - 1.5°C and radiation losses is maximum of 40%, then it can be shown that

$C_1 = 6.8$.

Evaluating C_2 (constant of correlation for turbulent flow)

According to the tests carried out, and FE predicted heat transfer coefficient curve and Hardisty et al [31] the distance exponent m = 0.4 for forced convection turbulent flow. Then it can be shown that; { $C_2 = 13.8$ } yielding the correlation:-

$$h_c = 6.8 + 13.8 \left(\frac{V^{0.8}}{X^{0.4}}\right) \quad (3.29)$$

The above correlation formula was programmed into the FE (ANSYS) model with appropriate conductivity values and noting the distances from the leading edge of the test board and 1/2 package pitch. The h values obtained from the correlation (equation 3.29) and those predicted by the FE model are illustrated in Figure 3.15b. A comparison of h values evaluated by the correlation formula (equation 3.29) and those of Wills correlation (equation 3.25) at two different datum points on the test board

(distance from the leading edge and the first row of package) is illustrated in Figure 3.15c.

As already mentioned and expected, the h values obtained in this research work are much higher than those evaluated by Wills [30] (equation 3.25). The discrepancy obtained was mainly due to the layout of the packages which was different in both cases. The resistance to air flow is lower with packages length parallel to the direction of the flow causing less turbulence and resulting in lower heat transfer coefficients.

3.10.6 HEAT TRANSFER CORRELATION UNDER AN IMPINGING JET

This phenomenon is clearly one of forced convection. Therefore, according to the classical forced convection heat transfer approach, a group of dimensionless parameters can be correlated using equation 3.18.

In this research, it is assumed that the existence of turbulent air flow in the test rig is due to the high turbulence in the jet and the roughness of the heat transfer surface. According to Liepmann [54], surface roughness produces immediate transition from laminar to turbulent flow when $\tau > 0.92\delta$. Vickers [48] estimates that the critical Reynolds number at which a round jet becomes turbulent is in the range of 1000 to 2000. Since in these experiments, even at low velocities the Re>1000 the jets over the packages are in a turbulent state.

A series of tests was carried out at different power dissipations (1.1765, 1.988, and

3 Watts/chip) and air velocities ranging from (1 - 4 m/s). The package temperature measured above the inlet air temperature for typical values mentioned above, are illustrated in Figures 3.16a, 3.16b and 3.16c.

The method of using the FE model described in section 3.9.2; to determine the heat transfer coefficient from the experimental data was similar to that described above. For a fixed value of power dissipation and of ambient temperature, the FE model was run with a series of different heat transfer coefficients. For a particular h value, the temperature difference between a point on the package corresponding to experimental thermistor measurement under package, representing the surface temperature and the ambient temperature was extracted from the FE data. Figure 3.16d illustrates h against temperature for particular power dissipations used above. Although various FE runs were carried out to predict the curves in Figure 3.16d, it was only necessary however, to determine one of the three curves shown in this Figure. The other two curves could be generated by increasing the temperature difference at constant h in proportion to the power dissipation. This procedure can be justified by the fact that when the heat transfer coefficient is constant, the thermal resistance of the package is constant. Under these conditions all temperatures increase in proportion to power dissipation [55].

The experimental data were correlated and the values of C and m were determined by plotting the Nusselt number against Reynolds number on log-log scale for all the experimental data Figure 3.17. A straight line least-squares fit using the graphical/statistical package (Sigmaplot) determined the values of the unknown

coefficients, yielding the required value of C = 0.0657 and m = 0.83 yielding the correlation:-

$$Nu = 0.0657\ (Re)^{0.83}\ (Pr)^{0.33} \tag{3.30}$$

For air, Pr number has almost a constant value of 0.7079 for a wide range of temperature and pressure, hence it is assumed constant. Analysis of the correlation in equation 3.30 for a typical test condition revealed a good agreement between the experiment and FE prediction ± 12% Figure 3.18. When comparing the evaluated heat transfer coefficients from equation 3.30 with those of Colburn [56] (turbulent boundary layer equation 3.31):-

$$Nu = 0.0292\ (Re)^{4/5}\ (Pr)^{1/3} \tag{3.31}$$

The results show that the evaluated heat transfer coefficients from equation 3.30 are about 40 - 50 percent higher with Reynolds number as low as 10^3. This evidently indicates that:-

1) The position of the thermistor for measuring the surface temperature is not suitable and a more accurate surface temperature measurement is required.
2) Vertical impinging flow, rather than parallel flow, can bring about higher heat transfer coefficient.

Another correlation formula according to Huang [58] has the form:-

$$Nu = 0.0233\ (Re)^{0.87}\ (Pr)^{0.33} \tag{3.32}$$

When comparing the heat transfer coefficients evaluated by equation 3.31 Colburn [56] with equation 3.32 Huang [58], it is evident that the measured values of heat transfer coefficient by Huang [58], are about 25 - 30 percent higher than those by Colburn [56].

When comparing the h values evaluated by equation 3.30 with those of Huang [58], the discrepancy of 25 - 40 percent is mainly due to the already mentioned surface temperature measurement position and test conditions.

When the evaluated h values from equation 3.31 [56], are compared with Kern [57], equation 3.33, empirical equation of fully developed pipe flow for gas oil heating:-

$$Nu = 0.0115\ (Re)^{0.9}\ (Pr)^{.33} \tag{3.33}$$

The heat transfer coefficients evaluated from equation's 3.31 [56] and 3.32 [58] are 20 - 40 percent higher than those derived from equation 3.33 [57], with Reynolds number 10^3 to 10^4.

3.11 CONCLUSION

The objectives set in this part of the research were fulfilled. One of the objectives achieved was the thorough evaluation of the test rig and the surface temperature measurement technique. Although the test rig was redesigned and improved the thermistor measurement technique was found to be limited.

The forced convection cooling of printed circuit board, with package orientation perpendicular to the direction of the flow, was investigated with special emphasis on the measurement and prediction of heat transfer coefficients along the PCB. The finite element method provided a superior tool to other numerical methods available. The FEM also avoided the need to make simplifying assumptions, when formulating the theoretical model which would have prejudiced the accuracy of the results.

Due to surface temperature measurement problems, the heat transfer of high speed impingement jet flow in cooling of printed circuit boards was not thoroughly explored. The problem of single jet impingement has often been treated by applying the theoretical analysis of forced convection heat transfer. To define those dimensionless groups in equation 3.18 in terms of different hole diameter and impact velocity would provide more data about such systems. The need for a better instrumentation for surface temperature measurement is of an essence for this type of study.

VELOCITY M/S	POWER (W)	T_{in} ∘ C	T_{out} ∘ C	m kg/s	ΔT CALC.	ΔT EXP.	% DIFF.
2	22.024	21	23.3	0.01115	1.97	2.3	16.7
"	29.976	"	23.7	"	2.68	2.7	0.7
"	39.153	"	24.2	"	3.5	3.2	-8.5
"	49.553	"	25.3	"	4.4	4.3	-2.2
"	61.176	"	26.4	"	5.46	5.4	1.1
3	22.034	19.5	20.4	0.01915	1.14	1.2	5.2
"	29.976	19.2	20.9	"	1.56	1.7	8.9
"	39.153	20	22.1	"	2.03	2.1	3.4
"	49.533	20	22.8	"	2.57	2.8	8.9
"	61.176	20	23.7	"	3.18	3.7	16.3
4	22.034	19.9	20.5	0.02642	0.83	0.6	-27.7
"	29.976	19.9	20.8	"	1.13	0.9	-20.3
"	39.153	19.9	21.1	"	1.48	1.2	-18.9
"	49.533	20.5	22.2	"	1.87	1.7	-9.0
"	61.176	20.5	22.7	"	2.30	1.9	-17.4
5	22.034	20.5	21.0	0.03370	0.65	0.5	-23.0
"	29.976	20.5	21.4	"	0.89	0.9	1.7
"	39.153	20.5	21.6	"	1.16	1.1	-5.1
"	49.533	20.5	21.9	"	1.46	1.4	-4.1
"	61.176	20.5	22.3	"	1.81	1.8	-0.5

TABLE 3.1- SUMMARY OF MEASURED EXPERIMENTAL CUMULATIVE TEMPERATURE RISE AND THEORETICAL CALCULATIONS USING ENERGY BALANCE EQUATION

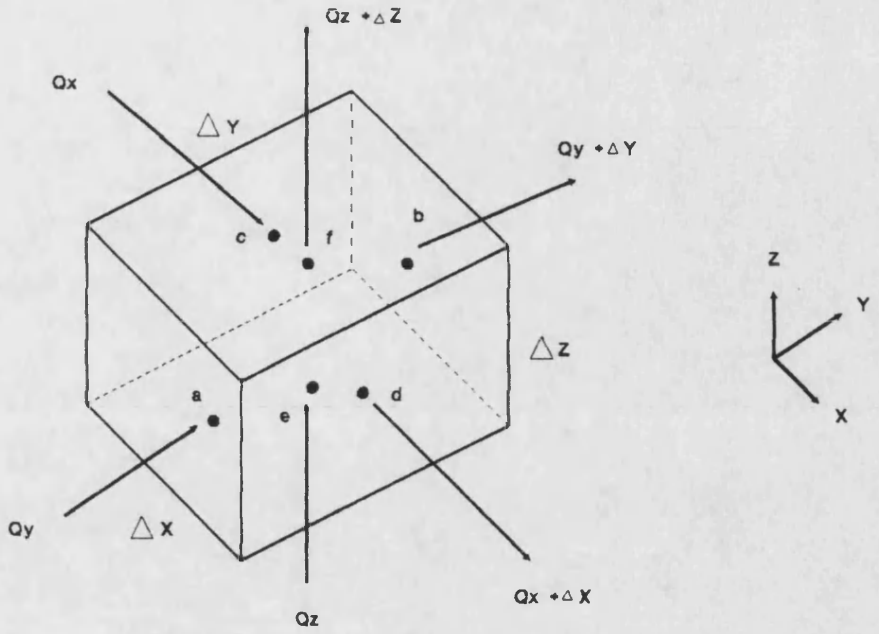


FIGURE 3.1a - VOLUME ELEMENT USED IN HEAT BALANCE

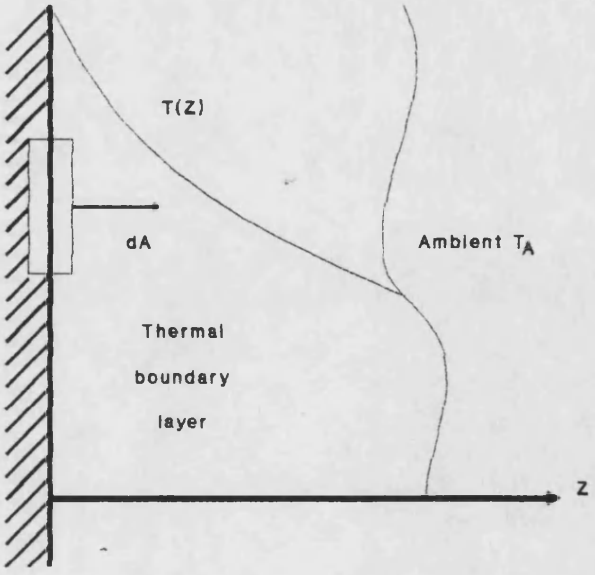


FIGURE 3.1b - HEAT CONVECTION AT A SOLID-AIR INTERFACE

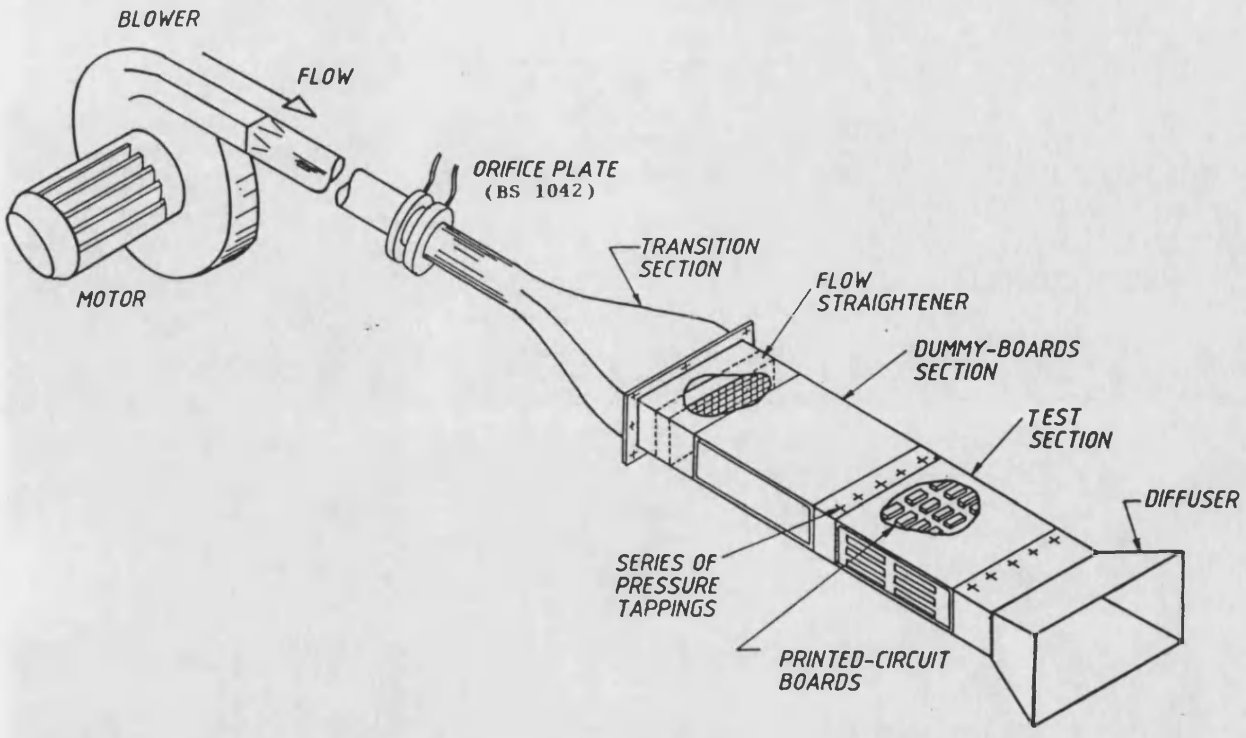


FIGURE 3.1c - GENERAL ARRANGEMENT OF RESEARCH RIG

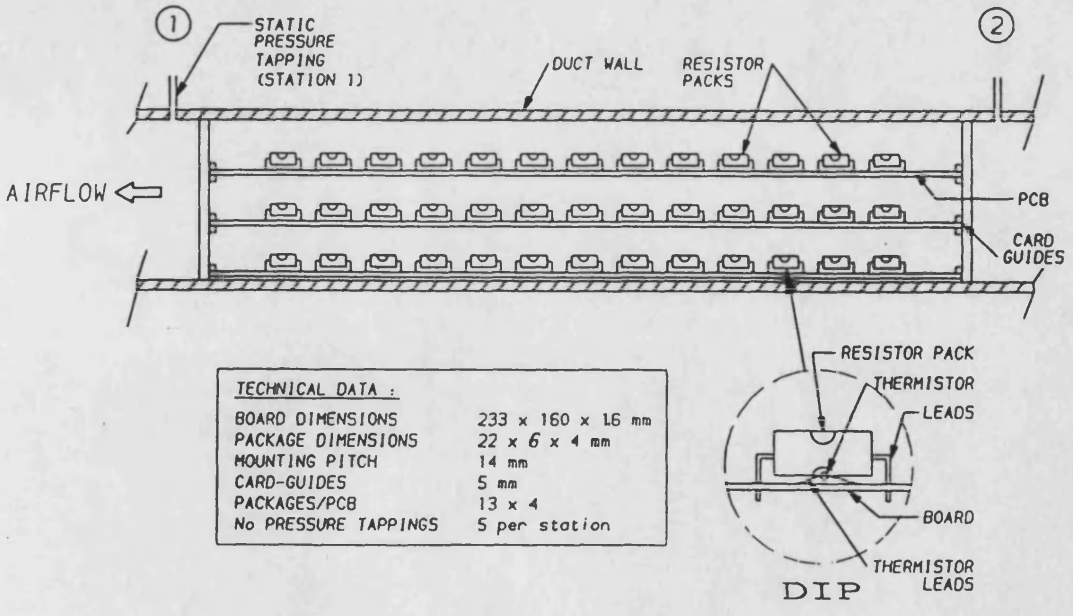
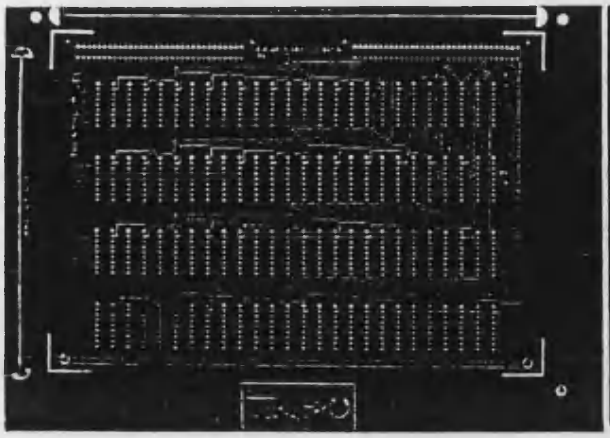
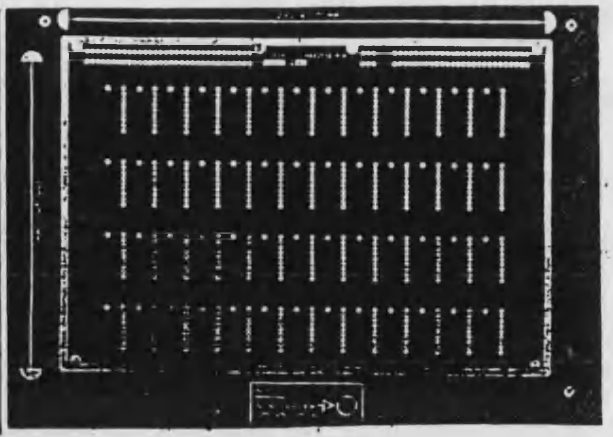


FIGURE 3.2 - TEST SECTION OF RIG

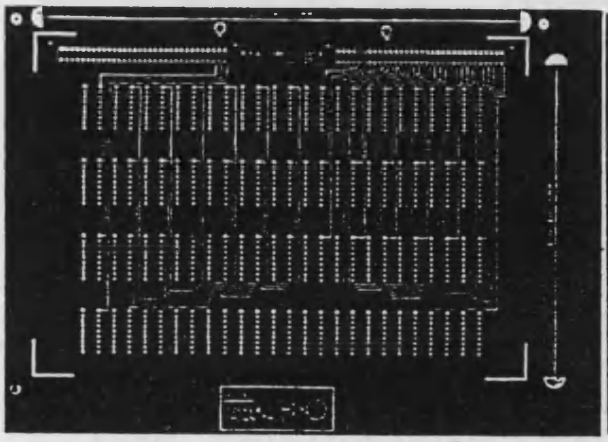
ARTWORK OF THE FOUR COPPER LAYERS



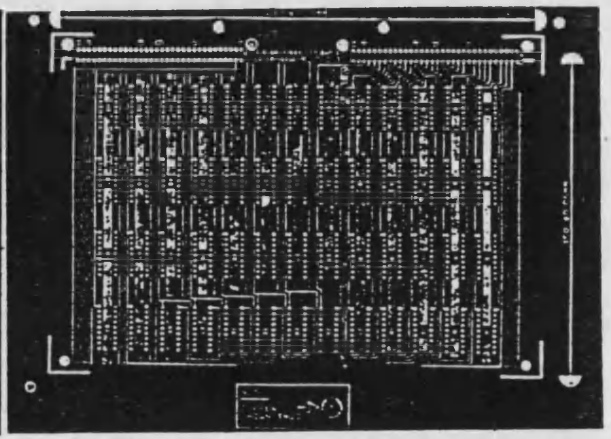
COPPER LAYER (1) - 50%



COPPER LAYER (2) - 90%



COPPER LAYER (4) - 25%



COPPER LAYER (3) - 75% copper

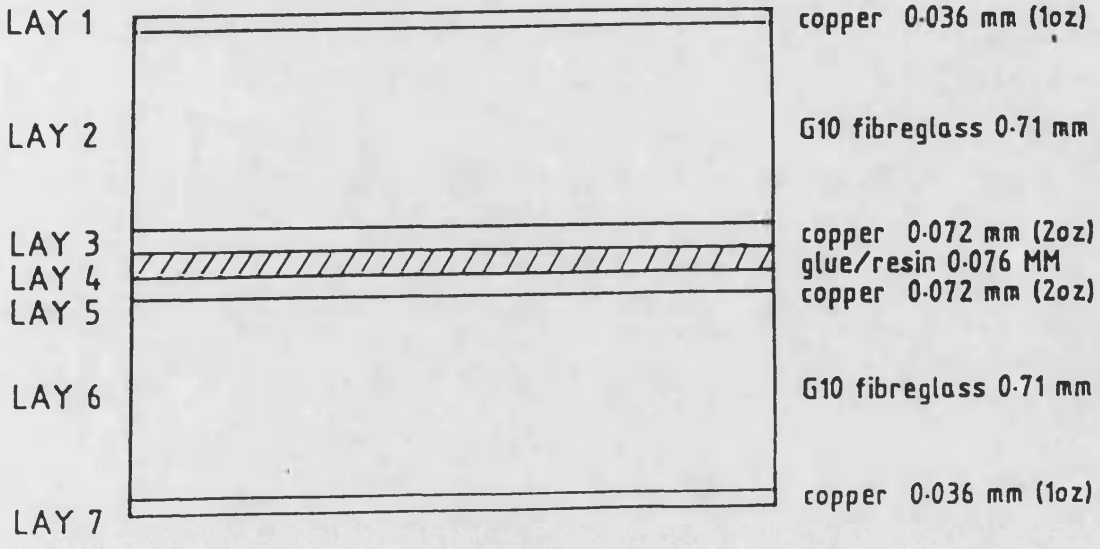


FIGURE 3.3 - CONSTRUCTION OF TEST PCB

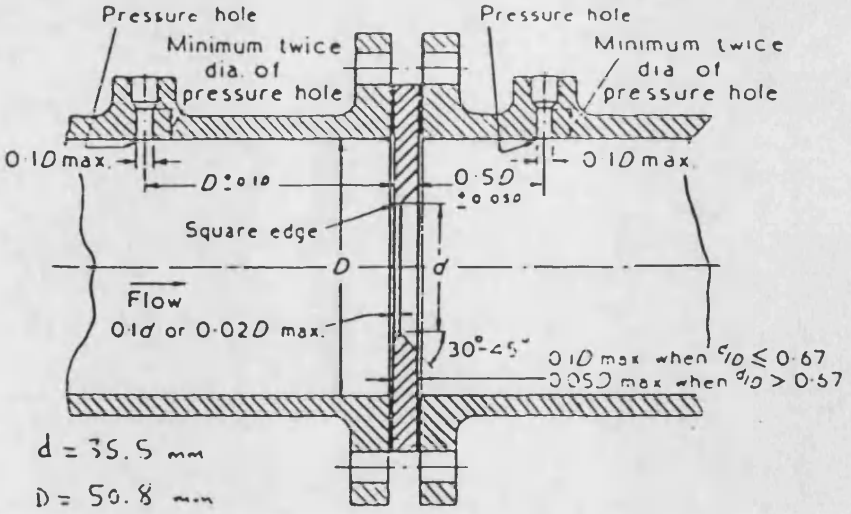
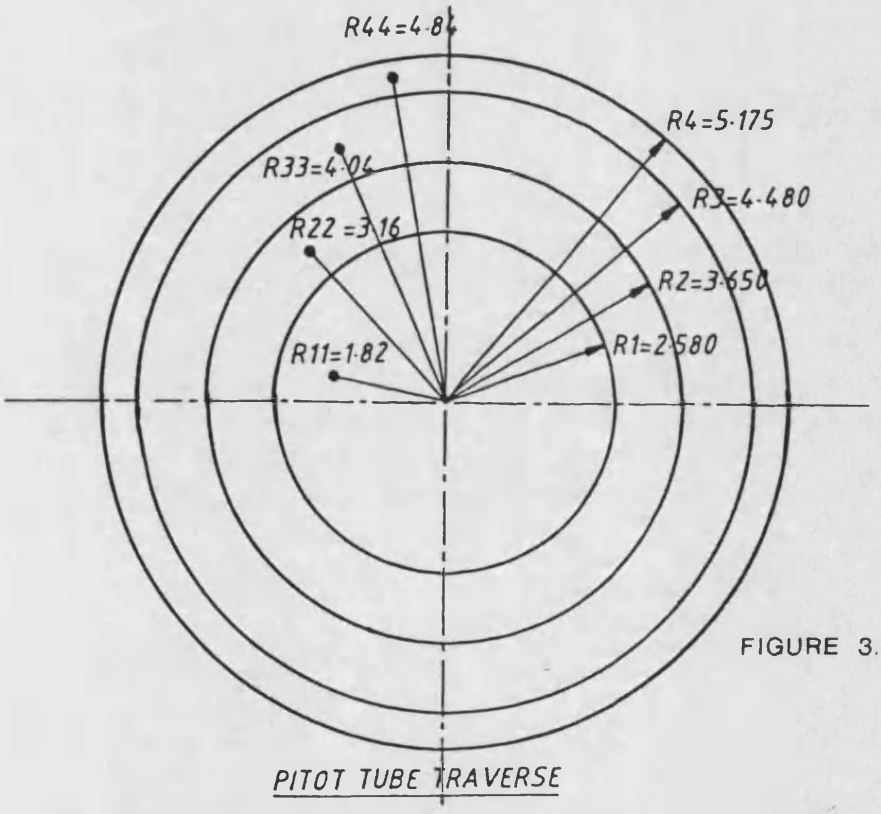


FIGURE 3.4a - ORIFICE PLATE WIDTH D AND D/2 TAPPING



$2R = 10.35$ cm

$R = 5.175$ cm

$\Sigma A = \pi R^2 = 26.78.$

$\frac{26.78\,\pi}{4} = 6.69\,\pi$

e.g.

$6.69\pi = \pi R11^2$

$R11 = 1.82$ cm

FIGURE 3.4b - POSITIONING OF PITOT TUBE IN PIPE

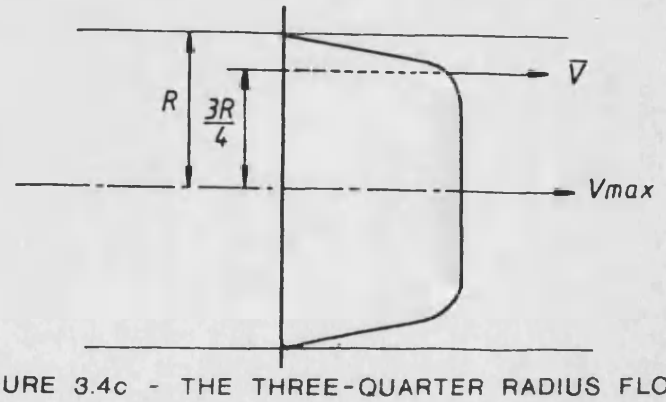


FIGURE 3.4c - THE THREE-QUARTER RADIUS FLOWMETER

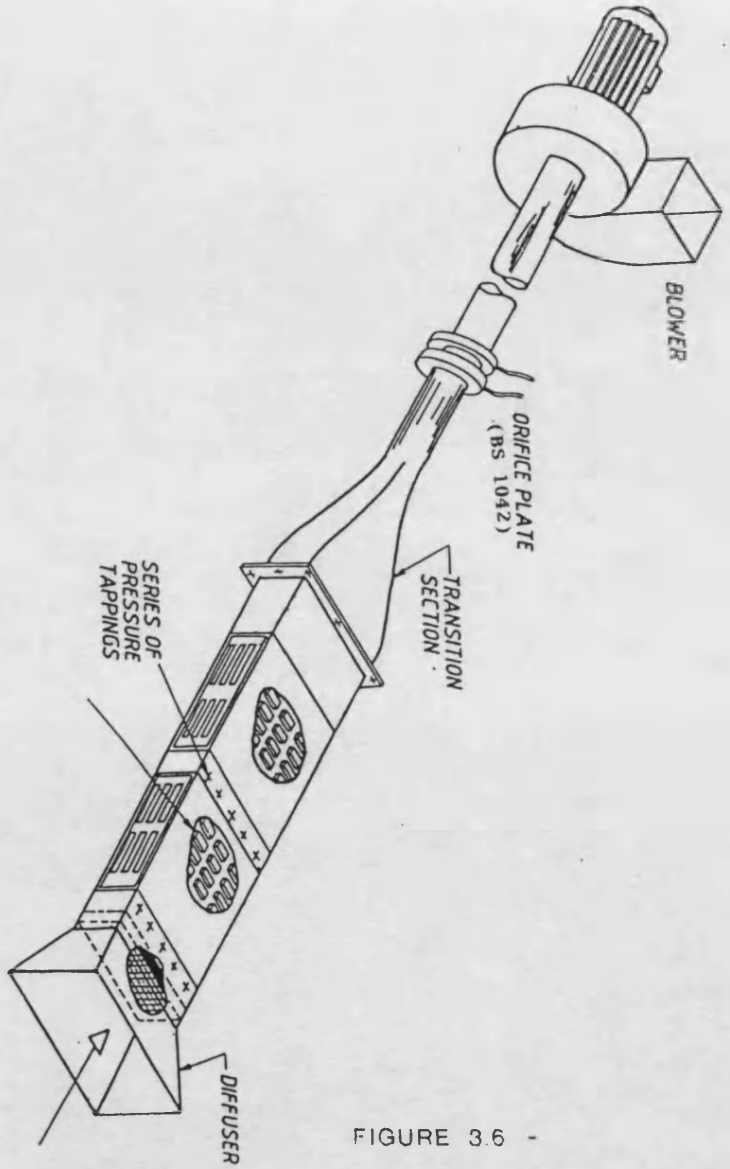


FIGURE 3.6 -

SCHEMATIC OF THE GENERAL ASSEMBLY OF THE RIG

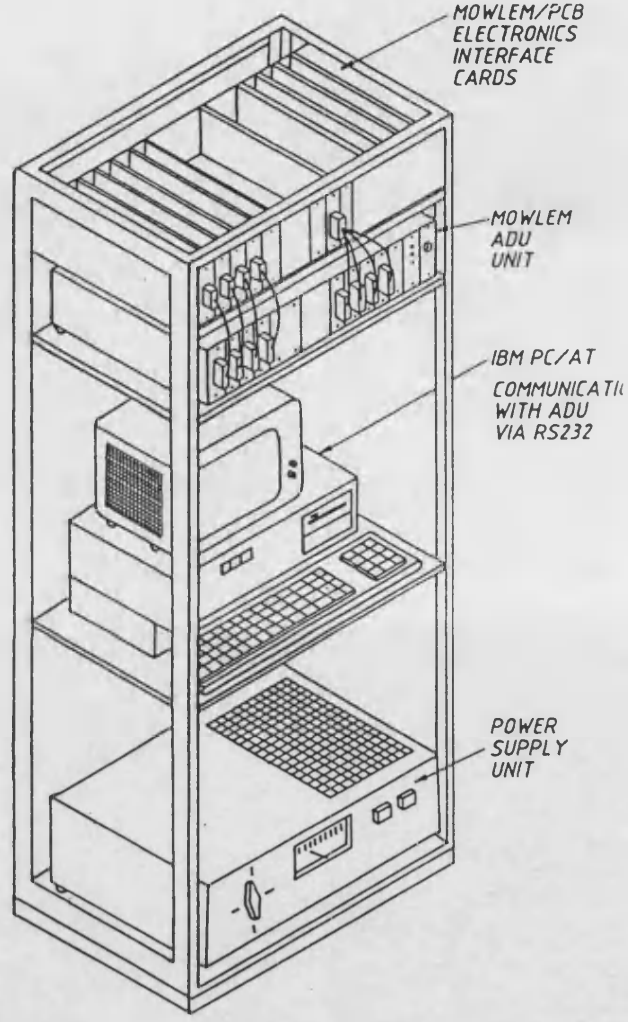


FIGURE 3.5 -

SCHEMATIC OF DATA ACQUISITION SYSTEM COMPONENT

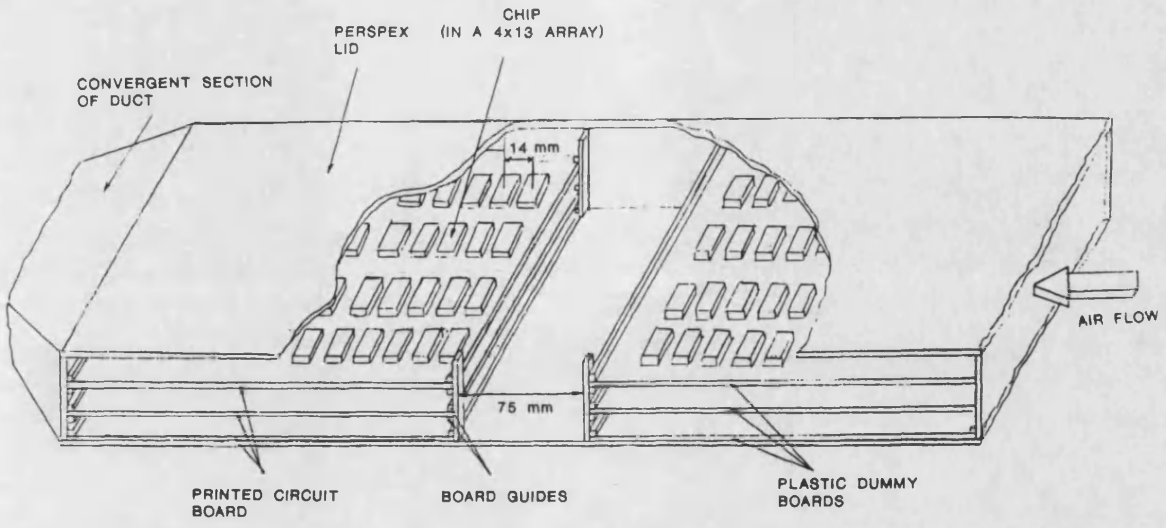


FIGURE 3.7a - TEST SECTION OF RIG - SCHEMATIC VIEW

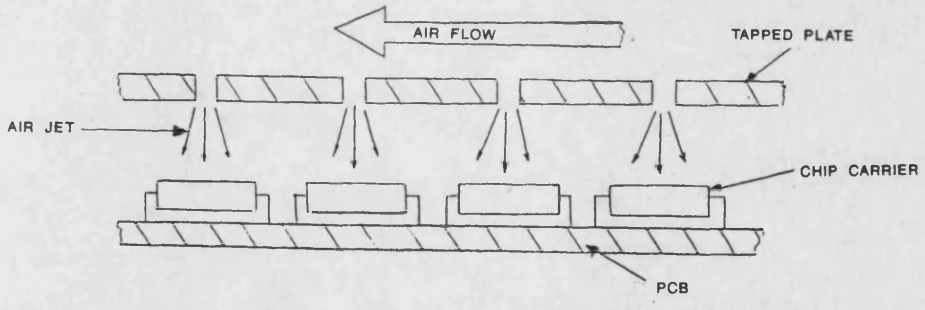


FIGURE 3.7b - COOLING OF CHIPS USING JET PLATE

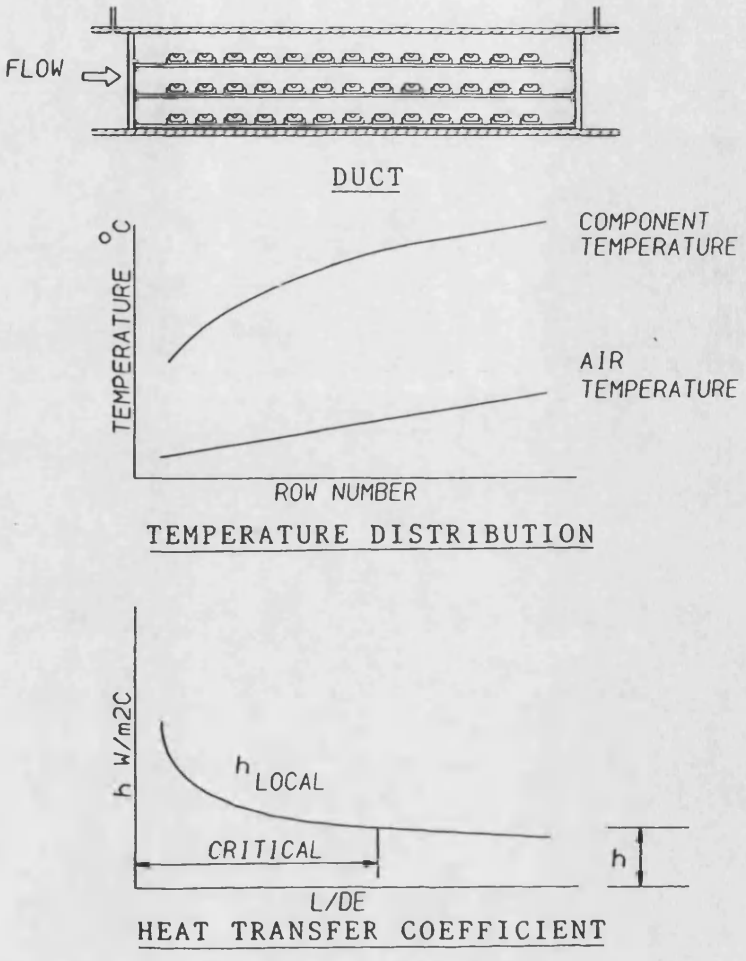


FIGURE 3.8a - FUNCTIONAL RELATIONSHIPS ALONG A DUCT

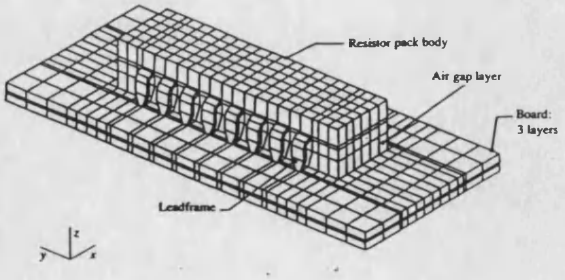


FIGURE 3.8b - FINITE ELEMENT MODEL II

FIGURE 3.9

INVESTIGATION OF THE THERMAL BOUNDARY LAYER

VELOCITY = 4 M/S POWER 0.5 W/CHIP

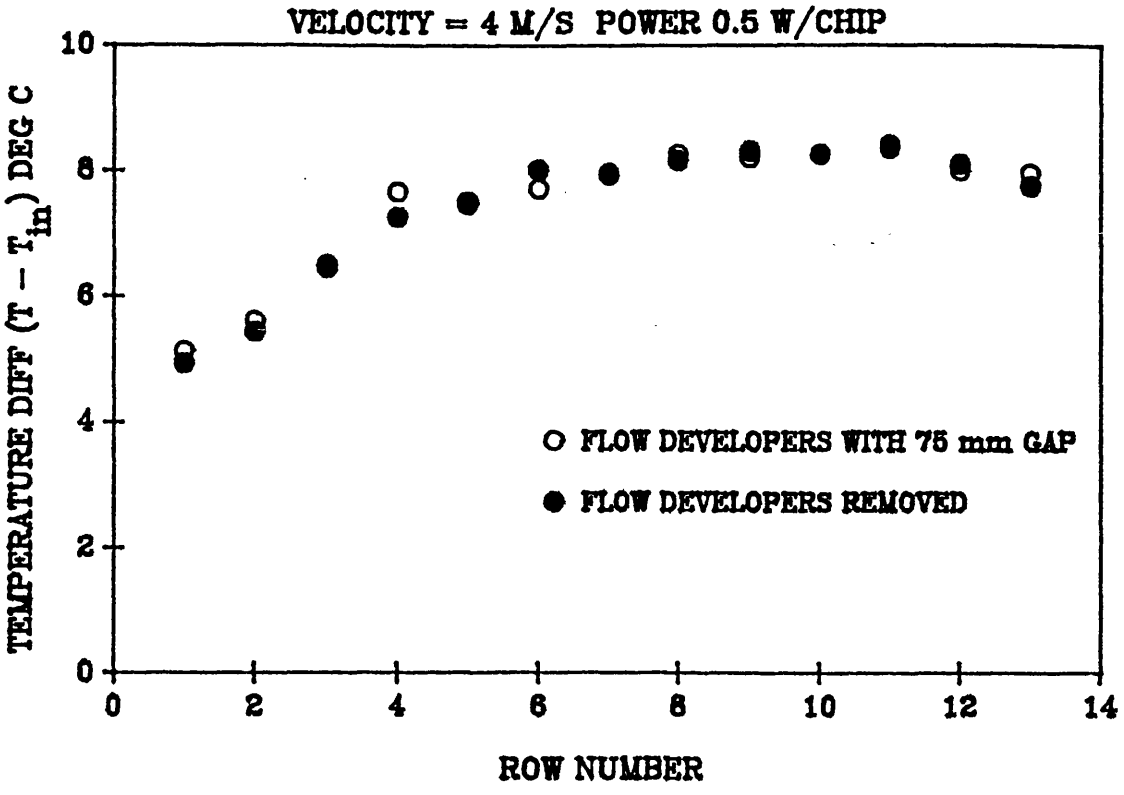


FIGURE 3.10

INVESTIGATION OF THE THERMAL BOUNDARY LAYER

VELOCITY = 4 M/S POWER 0.5 W/CHIP

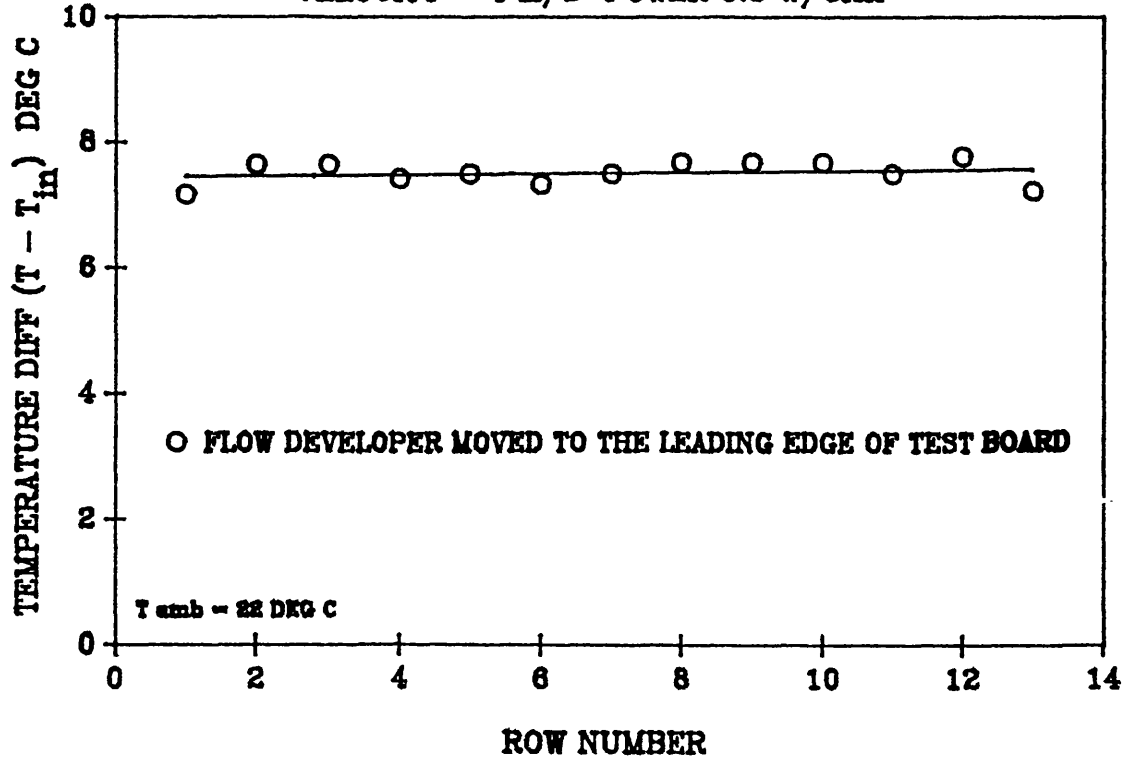


FIGURE 3.11a

TEST BOARD SET UP FOR THE BACK TO BACK TEST

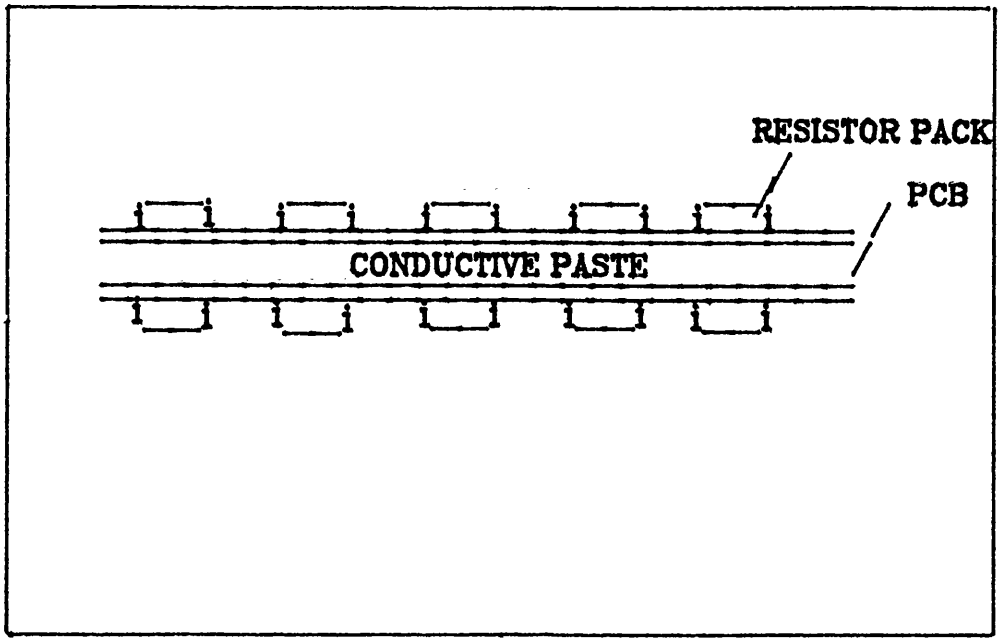


FIGURE 3.11b

PACKAGE TEMPERATURE DISTRIBUTION OVER THE TEST BOARD WITH AND WITHOUT HEAT LOSS FROM THE BACK OF PCB. POWER 0.7 W/CHIP VELOCITY 7 M/S

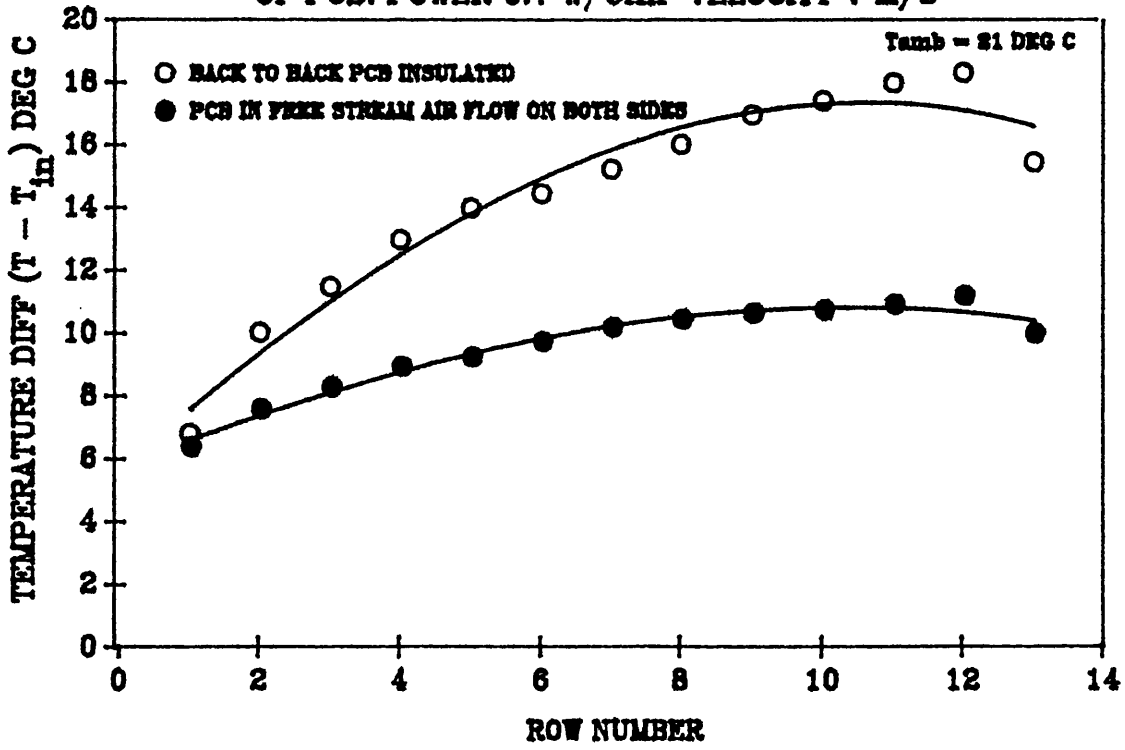


FIGURE 3.12

PACKAGE TEMPERATURE DISTRIBUTION OVER THE TEST BOARD WITHOUT HEAT LOSS FROM BACK OF THE PCB POWER 0.5 WATTS/CHIP

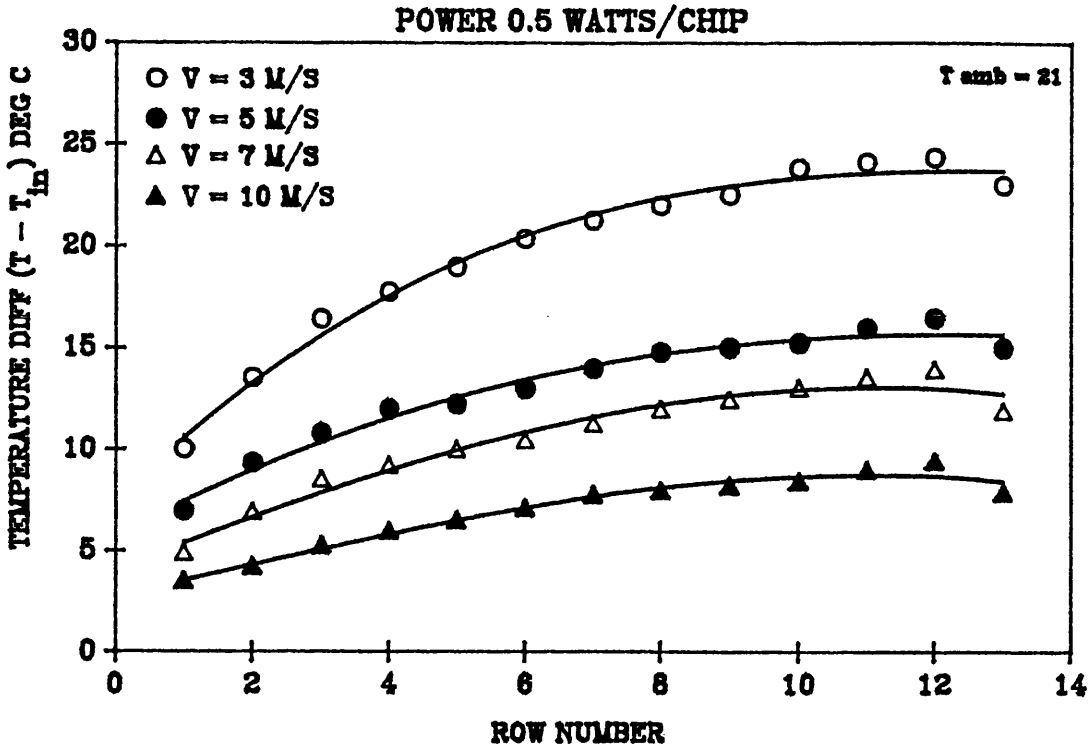


FIGURE 3.13

PACKAGE TEMPERATURE DISTRIBUTION OVER THE TEST BOARD WITHOUT HEAT LOSS FROM BACK OF THE PCB POWER 0.7 W/CHIP

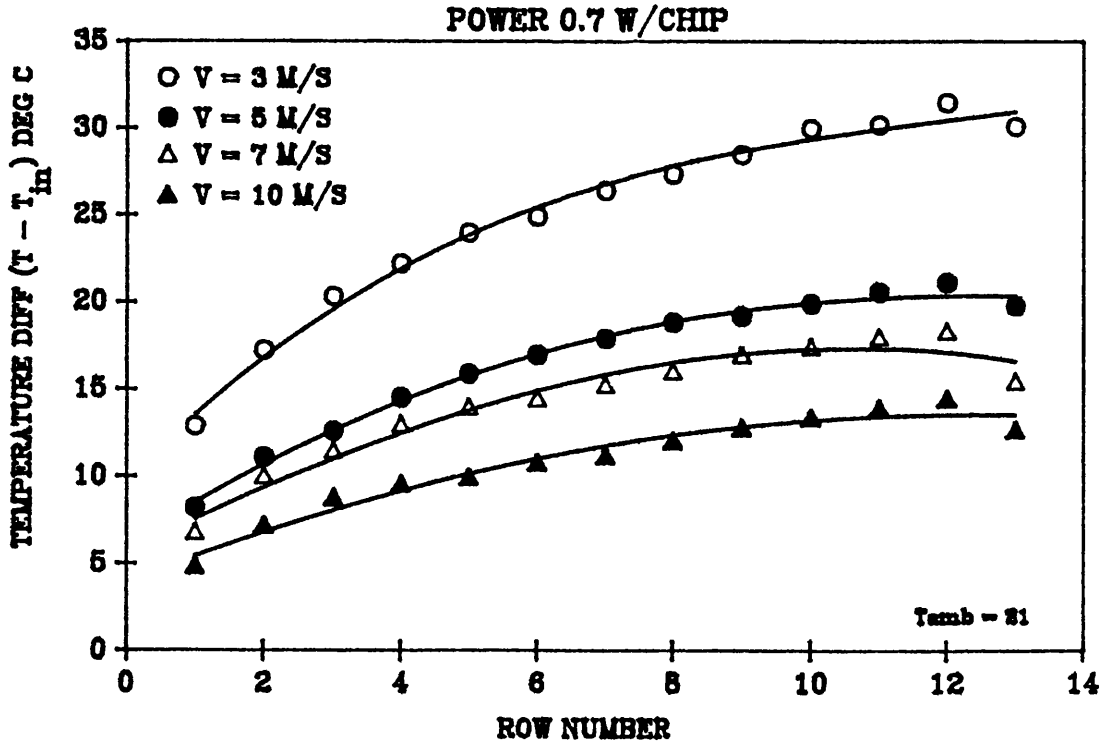


FIGURE 3.14a

HEAT TRANSFER COEFFICIENT VARIATION ALONG THE TEST BOARD
(UNIFORM POWERING AT 0.7 W/CHIP) VARIOUS VELOCITY

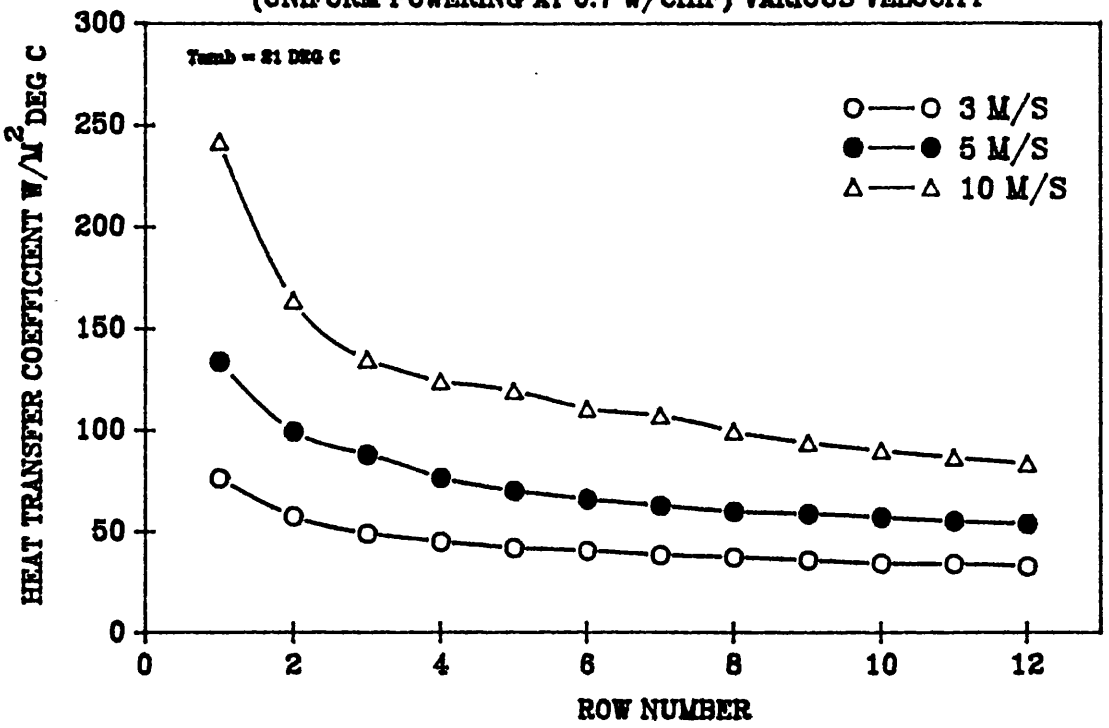


FIGURE 3.14b

COMPARISON OF FE PREDICTED AND THEORETICALLY
CALCULATED HEAT TRANSFER COEFFICIENT

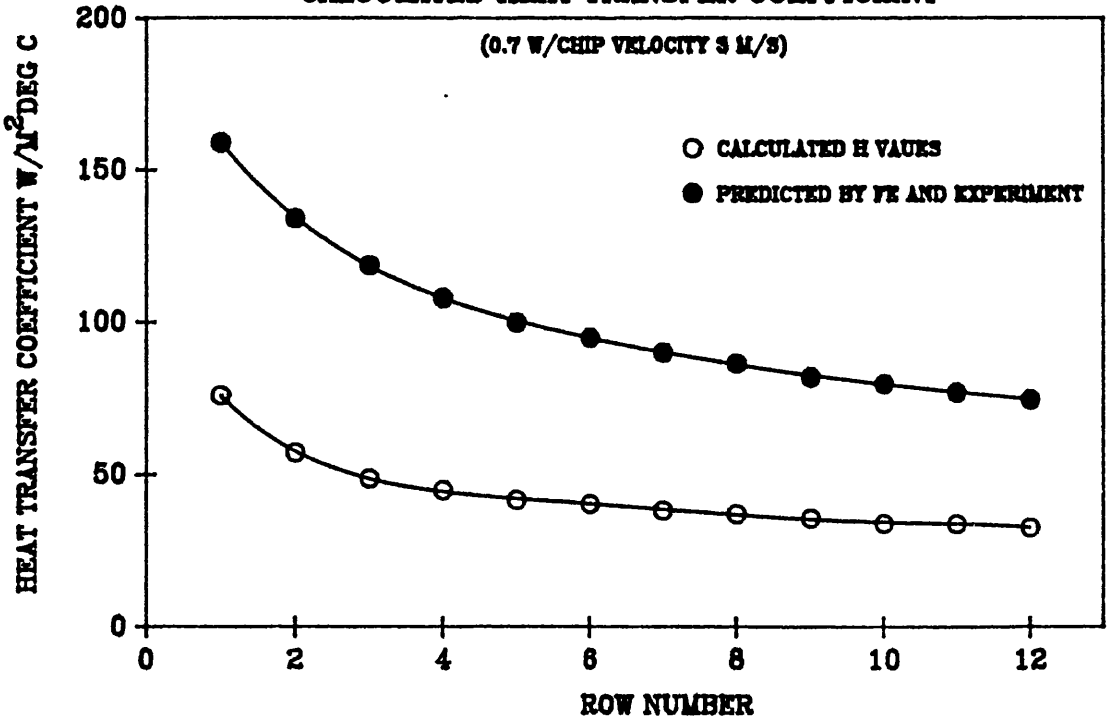


FIGURE 3.15a

HEAT TRANSFER COEFFICIENT VARIATION ALONG THE TEST BOARD (UNIFORM POWERING AT 0.7 W/CHIP) VELOCITY 3 M/S

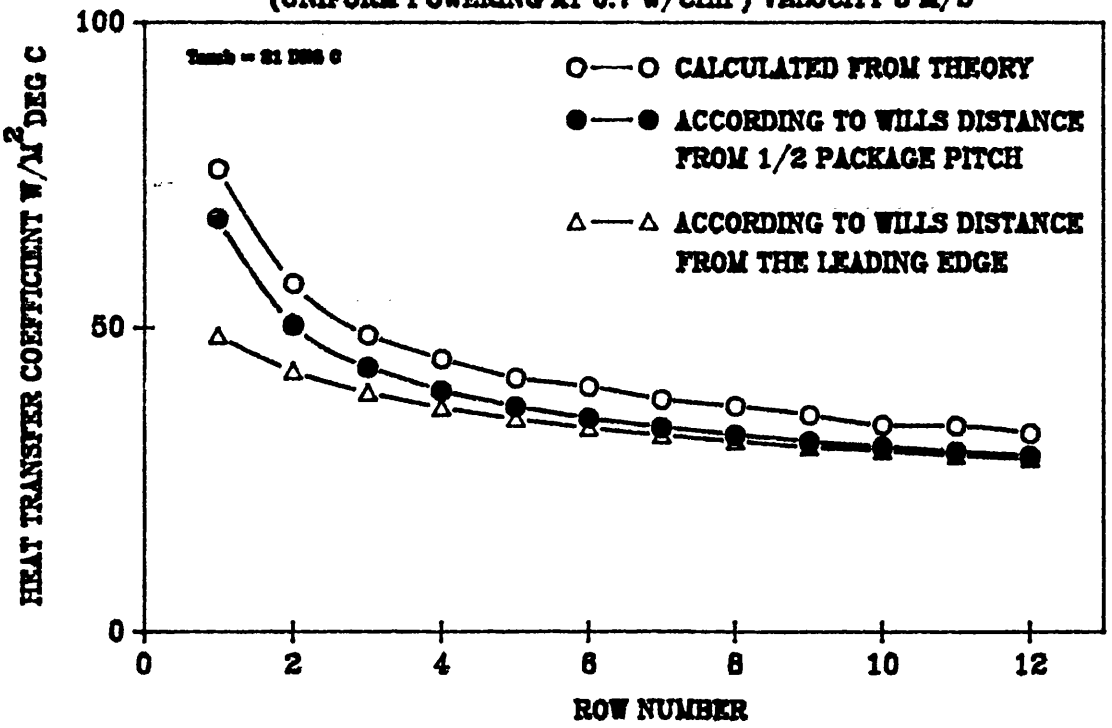


FIGURE 3.15b

FE PREDICTED AND CORRELATION EVALUATED HEAT TRANSFER COEFFICIENT POWER 1.1765 W/CHIP VELOCITY 2 M/S

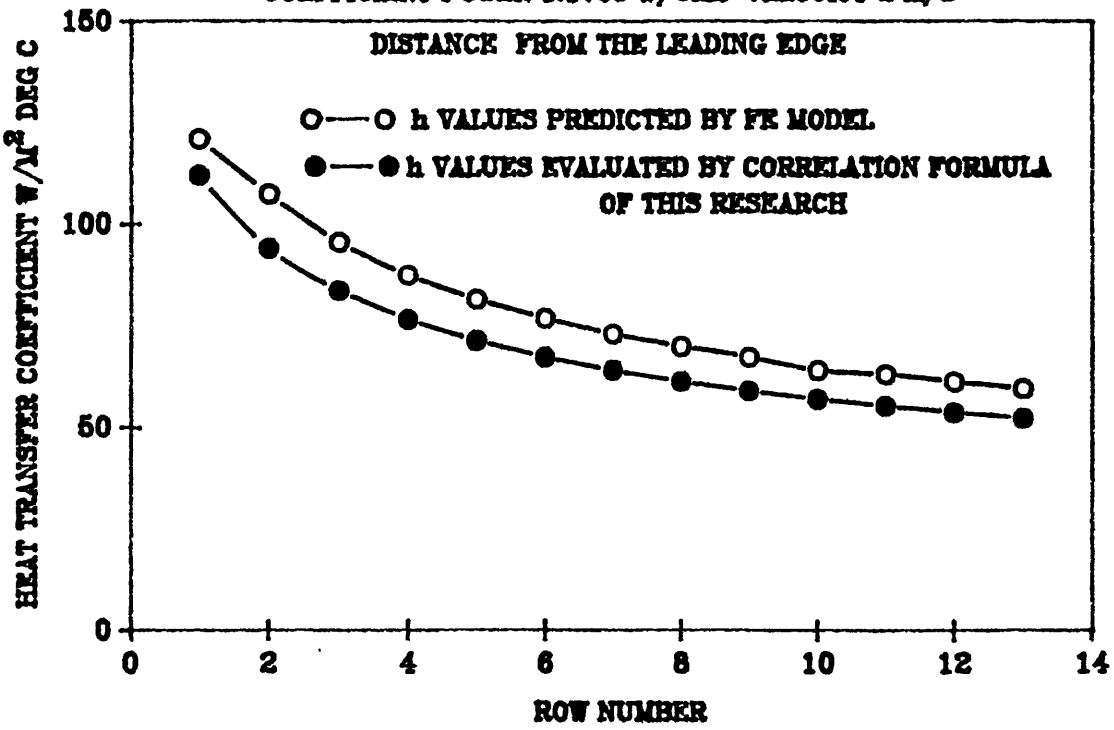


FIGURE 3.15c

COMPARISON OF h VALUES EVALUATED BY Eqn. 3.13 AND 3.15
POWER 1.1765 W/CHIP VELOCITY 2 M/S

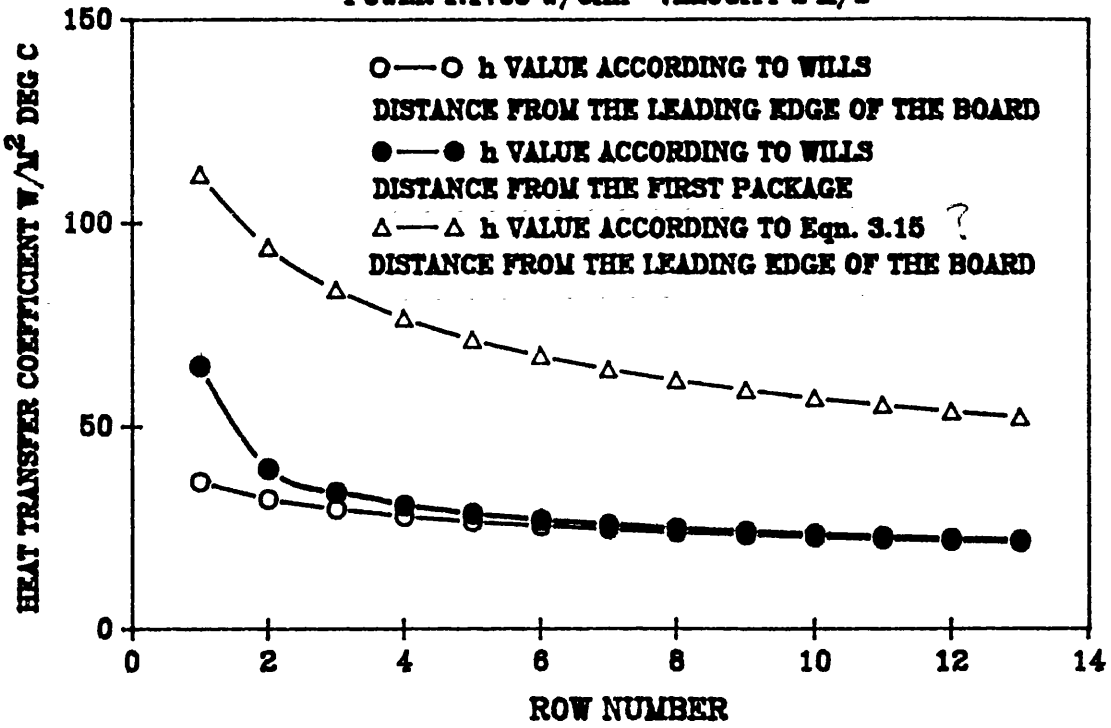


FIGURE 3.16a

COMPONENT TEMPERATURE DISTRIBUTION ALONG THE TEST BOARD
WITH IMPINGING–JET DIA. 2mm POWER 1.1765 W/CHIP

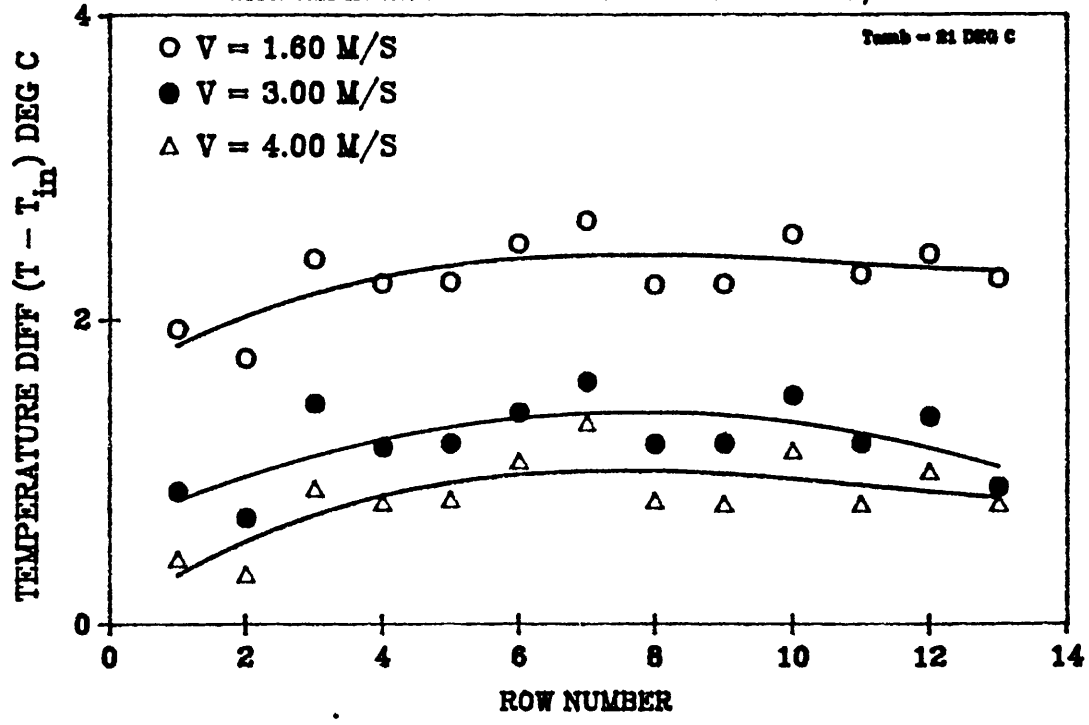


FIGURE 3.16b

COMPONENT TEMPERATURE DISTRIBUTION ALONG THE TEST BOARD WITH IMPINGING–JET Dia. 2mm POWER 1.988 W/CHIP

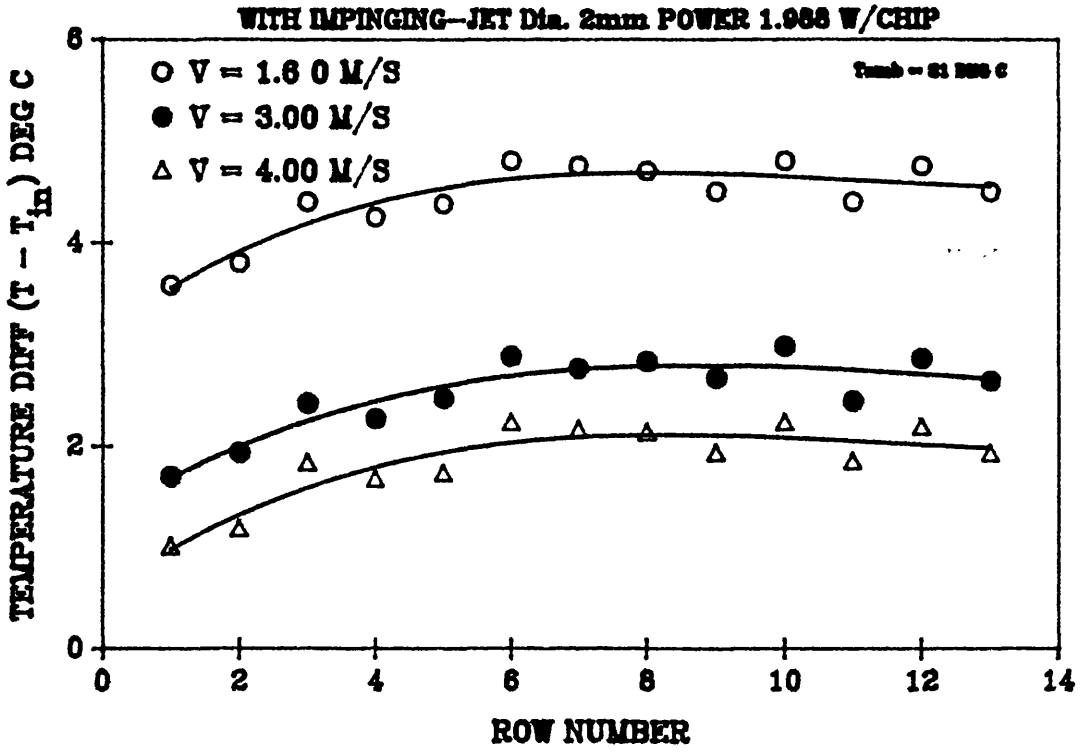


FIGURE 3.16c

COMPONENT TEMPERATURE DISTRIBUTION ALONG THE TEST BOAR WITH IMPINGING–JET Dia. 2mm POWER 3 W/CHIP

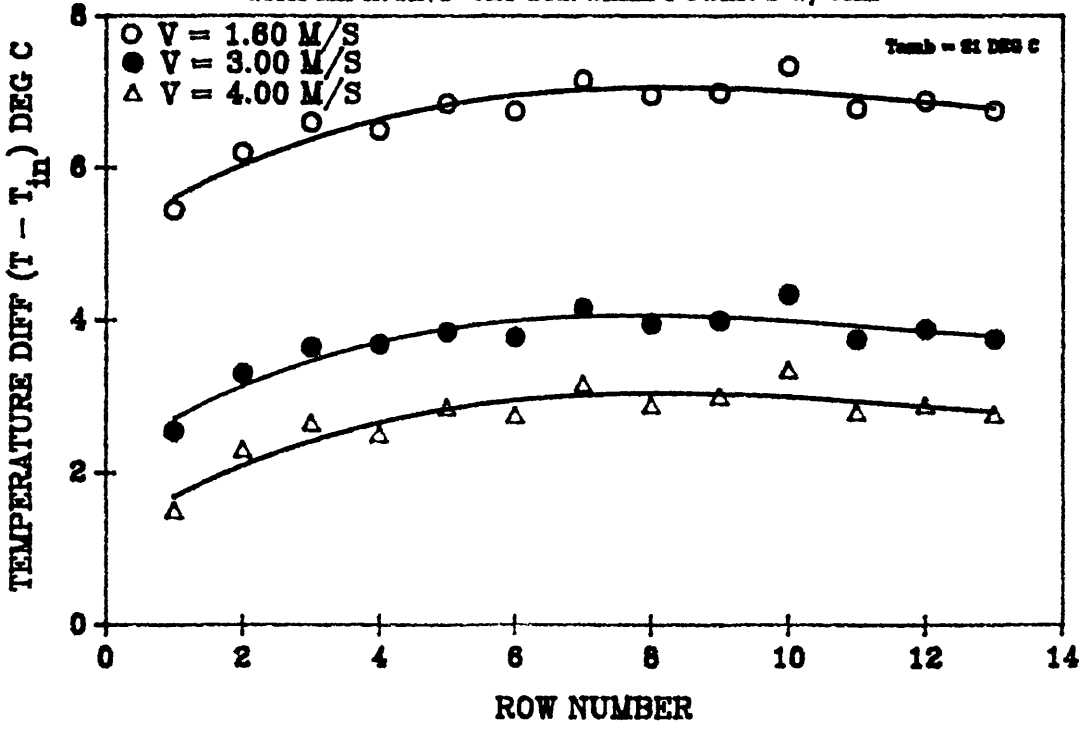


FIGURE 3.16d

COMPONENT SURFACE TEMPERATURE RELATION WITH HEAT-TRANSFER COEFFICIENT FROM THE FE MODEL

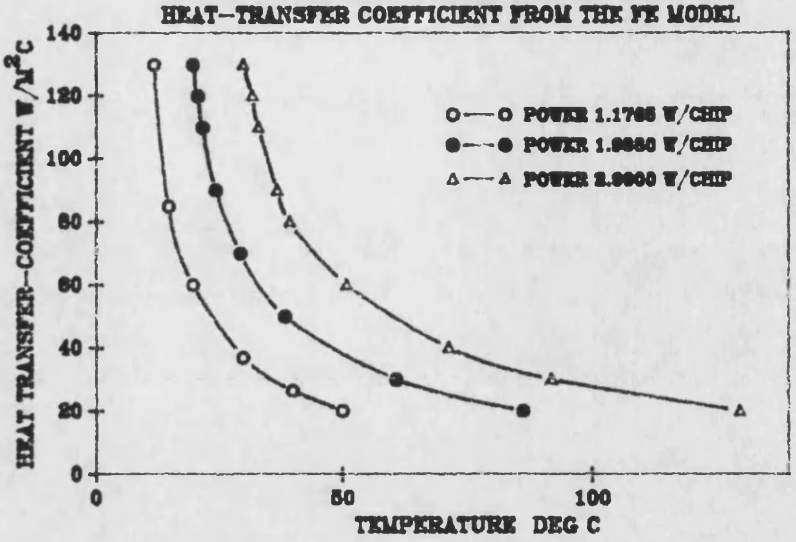


FIGURE 3.17

NUSSELT NUMBER AGAINST REYNOLDS NUMBER

CORRELATION FORM NU = C Re^{m} $Pr^{1/3}$

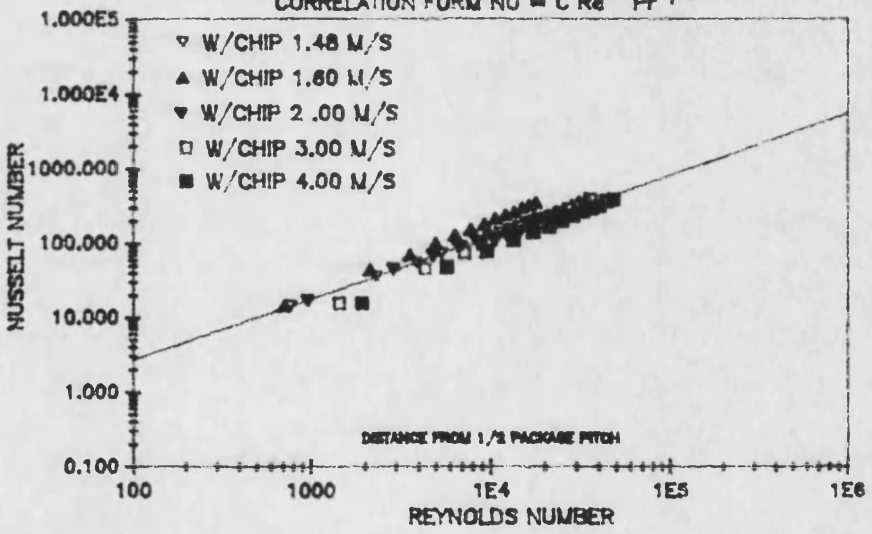
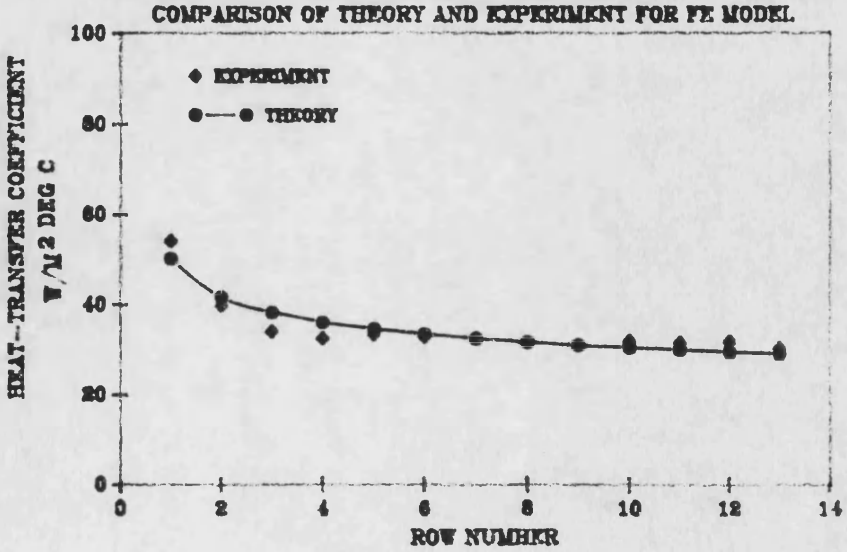


FIGURE 3.18

DISTRIBUTION OF HEAT-TRANSFER COEFFICIENT ALONG THE PCB COMPARISON OF THEORY AND EXPERIMENT FOR FE MODEL



CHAPTER 4

JUNCTION TEMPERATURE MEASUREMENT IN ELECTRONIC DEVICES

4.1 INTRODUCTION

Knowledge of the temperature within a solid body is required in many fields of technology but is of particular importance in experimental heat transfer investigations. Knowledge of surface temperature is a necessary starting point for the calculation of the heat transfer coefficient. In addition, the temperature reached during a process is required since it will in general affect the reliability or life of the product. Both of these aspects have relevance in the present research, since accurate determination of both junction temperature and surface temperature are necessary for an understanding of the complex heat transfer mechanisms involved.

Manufacturers of electronic components usually specify their thermal resistance R_θ and a maximum safe operating junction temperature $T_{j(max)}$. This specified thermal resistance is assumed to be constant for each device and is used to calculate the junction temperature as a function of power dissipation for a given mounting arrangement and ambient temperature. This information though useful, has limited application, as in a practical situation the mounting arrangements and ambient conditions vary from one system to another.

Although conventional methods using thermocouple and thermistors are relatively easy

to implement, they become impractical when applied to a miniaturised electronic package. In addition when attached to a surface they may cause flow disturbances in forced convection investigations, and also encounter problems of surface contact. Non-contact methods are preferred for surface temperature measurements, but these may introduce their own problems.

Temperature measurements using an infra-red (IR) instrument requires an uninterrupted line of sight, together with a knowledge of the emissivity of the surface under investigation. For research purposes, the emissivity problem may be overcome if the surface is painted black, ie. an emissivity of unity. Another common problem of the IR technique is the requirement of an viewing window transparent to IR when forced convection cooling is investigated.

An alternative indirect method of temperature measurement uses the characteristics of an on-board electronic component as a temperature sensitive parameter. This method is probably the only practical method of measuring the internal junction temperature in an actual chip. With this method, the measuring sensor is an integral part of the microelectronic system under investigation. No additional sensors or leads are introduced to interfere with the temperature field. Nearly all electronic packages possess a suitable component, in one form or another, which can be adapted to act as a resistance thermometer.

In this part of the research a complex electronic circuit was designed and developed, to measure the junction temperature of a DIP (SN7401) by forward biasing the

isolation substrate diode and measuring the voltage drop across it. Finite element modelling was also used to assist the validation of this technique.

4.2 RELEVANT LITERATURE

4.2.1 METHODS OF TEMPERATURE MEASUREMENT

As already mentioned in the introduction, the heat flow path within an electronic package is complicated. Reliable thermal data requires accurate measurements of the temperature field within the package. Conventional methods of temperature measurements are either unreliable or costly. An alternative to this problem is a purpose-built measuring instrument that can easily be implemented. This survey revealed only a few references to the on-board sensor method of temperature measurement.

Verster [59] describes a switching method, in which the collector current of the semiconductor is switched periodically between two fixed values. The ratio of voltage across the semiconductor junction under the two conditions is then only a function of a universal constant, and is a linear function of absolute temperature.

Mitchell and Berg [24] discuss the use of both electrical switching method and microscopy infra-red scanning for measuring the thermal resistance of a 16 pin DIP with design permutation and materials. The authors illustrate the difficulties encountered in measuring the case temperature of electronic devices.

Junction temperature measurement with a specially designed test chip is described by

Mclaughlin and Fitzroy [25]. Their thermal test chip houses thirty two transistors in 16 closely packed pairs, each of which can be powered individually to act as either a "resistance thermometer" or as a heat source. For a given power configuration, the IC temperature distribution can be determined by monitoring the temperature sensitive parameter "transistor". Although other authors, including Oettinger [60], reports the use of this technique, it is not a commonly used method of temperature measurement due to the high cost of manufacturing the thermal test chip.

Reich and Hakim [61] reviewed two methods of electrical switching technique for thermal resistance measurements, where the device was heated for 95-99% of the cycle and one of the three temperature sensitive parameters was monitored for (5-1%) of the cycle. They showed that thermal resistance is not constant over all ranges of voltage and current, and that the operating bias condition should be specified. Reich [62] described a continuous electrical method for thermal resistance measurement. The case-to-ambient thermal resistance, or other reference point (T_2) is evaluated, but he assumes that the reference point temperature is always less than the maximum junction temperature. The collector current (I_C) is set and a collector-base voltage (V_2) applied to the device. The temperature sensitive parameter **(TSP)** was measured under these conditions and then the reference temperature was reduced to a lower temperature (T_1) and the collector-base voltage increased to a value (V_1) until the same value of the TSP measure matched to the one as before. The thermal resistance was then calculated from the above values.

Although the investigations mentioned above, all have the same ultimate goal, the

methods used differ significantly from each other. The present survey also revealed further references to other methods of chip temperature measurement. These included liquid crystals, thermographic phosphors, laser scanners, liquid gas (bubble) formation techniques, and infra-red microradiometers [63-66]. Each of these techniques has its own set of problems ranging from cost effectiveness, spatial and temperature resolution, to ease of implementation and degree of contamination.

4.2.2 HEAT TRANSFER RESEARCH IN DIPS

Manchester and Bird [67] used a two dimensional network of thermal resistance to model conduction within a 16 pin DIP. For experimental measurements of internal resistance, external convective resistance (and variation in case temperature) were eliminated by immersing the package in a bath of liquid of uniform temperature. These authors also made a plea for standardisation of experimental methods of measuring thermal resistance. The effect of changing materials on the thermal resistance of 16 pin and 40 pin, plastic DIP's was investigated by Andrews et al [68]. Finite difference (network) packages were used for theoretical predictions of package temperature with good agreement between experimental and theoretical results, but few details of the network model was given.

Hannemann [69] has examined the various factors which influence package thermal resistance and has drawn attention to the difficulties of arriving at a simple, unambiguous definition of this resistance. The author has also discussed those tests conditions which must be standardised in order to reduce anomalies between

comparative resistance measurements on different packages.

4.3 TEMPERATURE MEASUREMENT ON MICROELECTRONIC PACKAGES

Conventional methods of temperature measurement, such as thermocouple and resistance thermometers, are not well suited to the task of making measurements on microelectronic packages for the following reasons:

a) The silicon die, the location of peak junction temperature, is inaccessible because it is totally sealed within the package.

b) Surface temperatures are inherently difficult to measure by contact methods. The sensor must form an integral part of the surface or an unknown contact resistance will be introduced. Because of the miniature nature of microelectronic packages, attaching a relatively massive sensor distorts the true temperature distribution.

c) An external sensor, together with its electrical connections interferes with the flow of coolant over the external surface of the package. Any interruption of the thin boundary layer will modify the values of the convective heat transfer coefficient.

4.4 SEMICONDUCTOR JUNCTION TEMPERATURE SENSOR (SID)

The substrate Isolation Diode (SID) is a standard electronic diode which is present in most electronic devices. The exceptions are silicon on sapphire, and dielectrically isolated devices. SIDs provide circuit protection by preventing damage caused by sudden reversal in the direction of current.

The voltage across the forward biased junction of a SID is temperature dependent and therefore the component can be used as a temperature sensor. The attraction of such a sensor is that it is actually mounted on the silicon. A significant disadvantage is that a complex high speed switching circuit is required to intermittently switch off power to the SID so that its voltage can be measured.

Both of the apparent disadvantages of non-linearity and device-to-device variability can be overcome by means of the electronic circuitry.

The methods which offer most accurate temperature measurement in a miniature electronic device are considered to be the on board sensor, the infra-red method and the thin film thermocouple. This latter method will be discussed in section 4.7 of this chapter.

Because silicon is a relatively good conductor of heat and the die is quite small, the temperature of the silicon and the integrated circuit on its surface, all have almost a uniformed temperature (to within 1 or 2° C) thus, for practical purposes, the signal from the SID is proportional to the "junction temperature" T_j, the maximum temperature of the module. The development and testing of a suitable circuit to sample and measure the SID voltage is described below.

4.5 OBJECTIVES

The main objectives of this part of the research are as follows:-

1) To assess the feasibility of a thin film thermocouple on the surface of a miniature electronic package for surface temperature measurement.

2) To determine the characteristics of a diode which formed part of a PCB specifically designed and manufactured for research.

3) Investigation of possible electrical measuring methods for junction temperature measurement of an electronic device, (continuous and pulsed method).

4) To design and develop a suitable high speed switching circuit which monitors the voltage drop across the substrate isolation diode (SID), with facilities to update and continuously display this voltage.

5) To establish a method of calibration.

6) To construct a realistic detailed FE model of the system to facilitate validation.

7) To validate experiments on a commercially available test chip (TTLSN7401 and SN74LSO1) against a finite element module of the system.

8) Use the combination of the SID and FE to investigate the internal and external conduction path in a commercial DIP (SN7401).

4.6 CONCEPT OF THERMAL RESISTANCE

The concept of thermal resistance has for many years been used by engineers, and electronic package manufacturers as an aid to calculate the junction temperature of a semiconductor. This concept is based on the analogy between the electrical and thermal properties of materials, with temperature, power dissipation, and thermal resistance being analogous to voltage, current, and electrical resistance, respectively. Therefore the thermal resistance (R_{JR}) is defined as:

$$R_{JR} = \frac{(T_J - T_R)}{P} \qquad (4.1)$$

where:-

R_{JR} = Thermal resistance between junction and reference point, °C/W
T_J, T_R = Temperatures of junction and reference point respectively, °C/W
P = Power dissipation in the device, W

If the reference temperature is that of the external surface of the package then internal resistance is calculated. If the temperature difference is that between surface and ambient then the external resistance is evaluated. For accurate determination of package temperature it was decided that surface temperature should be measured either by thin film thermocouple or infra-red methods, and that junction temperature should be measured by the SID technique.

4.7 DEVELOPMENT OF A THIN FILM THERMOCOUPLE

This method is based on the same principle as the conventional thermocouple, with the difference that, the thermocouple junction is a thin film deposited on the surface of the object. Almost any material that has the appropriate thermoelectric properties can be used in the thin film technique. Alumel and chromel, typical thermocouple materials, were used.

4.7.1 SPUTTERING PROCESS

This is a vacuum coating process whereby the material is dislodged and ejected from the surface of the target (cathode) due to bombardment of the surface by energetic

particles. The target and the substrate to be coated are placed in the vacuum chamber with the target directly above the substrate. The chamber is then evacuated to pressure of about 5 x 10^{-4} to 5 x 10^{-7} torr. The bombarding ions are generally the ions of heavy inert gas such as argon, krypton or xenon. The substrate is placed under the target so that it intercepts the sputtered atoms. Ion bombardment is provided by igniting an electric discharge in the vacuum chamber in order to ionize the inert gas close to the target surface. Such low pressure electric discharge is called glow discharge and the ionized gas is known as a plasma Figure 4.1a.

4.7.2 SPUTTERING ON TO THE SURFACE OF A DIP

Two wires of the target material to be used, chromel and alumel were attached to the extremes of the DIP surface in order to connect the thin film thermocouple to the voltage measuring instrument. The DIP was initially completely covered with aluminium foil. A 2 mm^2 area above the chip together with a thin connecting line to the attached wire were then exposed through the aluminium foil. A 37.5 minutes sputtering process was required with the alumel target to produced the desired deposit. The process was repeated for the chromel target. An overlap of 1 mm was allowed between the two regions to form the chromel/alumel junction, Figure 4.1b.

Although the technique was successful it had a significant disadvantage, which caused it to be abandoned. It was found that a period of some 75 minutes was required to sputter each thermocouple junction. This entailed that, for an array of 52 packages on a PCB, 3900 minutes would be required. This was not considered to be viable,

because of the high cost of running the sputtering equipment. For surface temperature measurement the non-contact IR method was considered to be more practical. The IR method will be discussed in greater detail later.

4.8 ELECTRICAL METHODS OF MEASURING JUNCTION TEMPERATURE

Electronic devices can not be characterised by a unique value of thermal resistance because of variations in cooling conditions and of mounting arrangement. It is therefore important to be able to measure the critical junction temperature for a range of operating and mounting conditions.

A number of electrical components, such as the forward-biased collector-base voltage (V_{CB}), The d-c forward current gain (h_{FE}), the collector-base leakage current (I_{CBO}), and the forward-biased emitter-base voltage (V_{EB}) can be used as a temperature sensitive parameter (TSP). The various techniques required for monitoring each of these parameters, can generally be classified as either:

a) Continuous methods.

Or as a

b) Pulsed or switched methods.

Each application requires the construction of an electronic circuit which will relate the output of the TSP to the junction temperature. The degree of difficulty in developing such a circuit is a major factor in assessing the worth of a particular technique. A brief

description of the use of the various electrical components as TSPs is given below, followed by a detailed description of an accurate preferred technique which most closely meets the requirements of the present investigation. A requirement of the circuit was that it had to be capable of measuring the temperature of the device during transient conditions.

4.8.1 CONTINUOUS ELECTRICAL METHOD

In this method the TSP is monitored while the test device operates at full power. With the continuous method it is assumed that the measured variable (h_{FE} or V_{BE}) will vary monotonically with temperature, also that any variation in output from the TSP caused by changes in its bulk temperature will be much greater than variations caused by changes in the collector-base voltage (V_{CB}). Unfortunately both h_{FE} and V_{BE} may be strong functions of V_{CB}, and it is often difficult to separate these electrical effects from the desired thermal effects. For example in the continuous V_{BE} method, a correction for these effects may have to be included [70-71]. The added complexity required for this correction negates the apparent simplicity of the continuous V_{BE} method.

4.8.2 PULSED OR SWITCHED METHOD

In this method the test device is rapidly switched between conditions of full power dissipation and very low or no power dissipation. The TSP is monitored during the short interval when the power is switched off. The TSP is calibrated by placing it in a temperature controlled oven with power switched off.

Since in some cases, due to amplification, h_{FE} can be a double valued function of temperature, it is not recommended for use as TSP. The switching method based on V_{EB} or V_{CB} as the TSP are both equally accurate. However, it has been found that V_{EB} method tends to indicate a junction temperature closer to the peak temperature than the V_{CB} method. Since, in addition, the electronic switching circuits are simpler for V_{EB} method, it was selected for use in the experimental investigations at Bath. With this objective electronic switching circuitry was designed and developed for IC temperature measurement.

4.9 CHARACTERISTICS OF A DIODE

A diode is formed from one of the transistor connections shown in Figure 4.2. For each of the configurations a, b, and c, forward-biasing the diode will result in current flowing in the substrate. This does not occur with the configuration (d) because the collector/base potential is maintained at 0 V.

In the early stages of the design of the pulsing board a simple diode network was constructed to establish the suitability of a diode as a TSP. The circuit shown in Figure 4.3a consisting of a diode, 10 K resistor, -10 volt power supply, was constructed on a standard PCB. The board was then placed in an oven, and the voltage drop across the diode was monitored, as the temperature of the oven was gradually increased from 0 to 100°C . The effect of this circuit was to forward bias the diode and to ensure low current in the circuit. The characteristic of the diode with increased temperature proved to be linear, as illustrated in Figure 4.3b.

4.10 EXPERIMENTAL METHOD - BACKGROUND HEAT TRANSFER

For most of the experiments, the experimental procedure was as follows. A single electronic module was suspended in the appropriate cooling environment, usually either natural or forced convection of air. The SID measuring system was activated to monitor the chip temperature. The power supply to the chip was set to some constant value, and then, at time zero, the power was switched on. Temperatures were monitored as the chip heated up to its equilibrium condition.

When power is supplied at a steady rate P (W/m^3) to a body of mass which is losing heat by convection to an environment at a constant temperature T_A, the temperature of the body T must satisfy the following energy balance equation:-

$$P\,V - h\,A\,(T - T_A) = m\,c_p\,(\frac{dT}{dt}) \qquad (4.2)$$

where:-

V = Volume of body, m^3
h = Heat transfer coefficient, W/m^2 K
A = Surface area of body, m^2
T = Temperature of body, °C
T_A = Ambient Temperature, °C
t = time, s

Before a simple solution of equation 4.2 is possible, a number of conditions must be satisfied. The body must be a good conductor so that the temperature T is uniform throughout the body, and, the heat transfer coefficient h must be constant.

Assuming for the present that these conditions are satisfied, then the system can be

treated as a lumped parameter system, and equation 4.2 may be solved to yield the temperature difference between the body and its surroundings [72]:-

$$\theta = \theta_m \left(1 - e^{\left(\frac{-t}{\tau}\right)}\right) \tag{4.3}$$

where:-

θ = $T - T_A$, °C
θ_m = Equilibrium value of θ (PV/hA), °C
τ = Time constant, ($\rho VC_p/hA$), s

When the temperature of the body cannot be considered to have a single uniform value, but the other assumptions still hold then equation 4.3 must be modified as follows:-

$$\theta = \theta_m \left(1 - e^{Bi\ Fo}\right) \tag{4.4}$$

where:-

Bi = Biot number (hl/k), dimensionless.
Fo = Fourier number ($\alpha t/l^2$), dimensionless.
α = Thermal diffusivity ($k/\rho\ C_p$), m^2/s

Thus during a test in which power is supplied at a constant rate the temperature difference θ should increase exponentially to a maximum value θ_m. The Biot number expresses the ratio of the internal thermal resistance of the body (conduction), to the external thermal resistance of the coolant (convection). The Fourier number is a dimensionless time scale.

4.11 DEVELOPMENT OF THE PULSING AND SWITCHING BOARD

The commercially available dual-in-line package, DIP, (Logic Module TTL SN7401 Quad Four input NAND gate open collector output) was selected as the test chip. The objective was to devise an operating cycle in which the power could be switched on for 99% of the time, and off for the remaining 1%. During the short off-period, a voltage applied to the substrate isolation diode involved would be used to measure its temperature. Because the power to the chip is switched off for such a small fraction of the operating cycle, the SID remains essentially at its operating temperature.

The TTL 7401 DIP was incorporated into the circuit shown in Figure 4.4. The circuit was developed to perform the following functions:-

a) Supply power to the logic gates of the TTL 7401.
b) Apply a forward bias to the SID.
c) Generate a suitable pulse form for switching.

During the initial tests, all inputs to the DIP were connected in common.

4.11.1 LOAD RESISTORS

Tests showed that to produce the required level of power dissipation it would be necessary to connect a pair of load resistors (100 Ω and 200 Ω) in series with each logic gate.

4.11.2 DELAY PERIOD

In order that the power voltage should not interfere with the measuring voltage, it was necessary to determine the delay time after switching-off for the power voltage to decay, Figure 4.4. Transient conditions were simulated by connecting a pulse generator, through an invertor, to the test chip. The exponential decay characteristic of the chip was recorded in an oscilloscope under conditions of full load and no load Figure 4.5.

4.11.3 SWITCHING THE TRANSISTOR AND FORWARD BIASING THE SID

Having established the transient characteristics of the chip, the inputs were un-commoned. The pulse generator was then connected, through the invertor, to the transistor which acts as a switch. When point B in the circuit is at zero volts (for 99% of the cycle) the switch is closed, and the chip is powered from the 5 Volt bus. The effect of an "off-pulse" is to produce 5 volts at B, and to switch off power to the chip. The SID is then forward-biased, and current flows through it from the ground to the -10 volts potential.

4.11.4 TIMING AND PULSING CIRCUIT

This circuit replaced the pulse generator used in preliminary tests. A standard 555 timer, operating in astable mode, was selected to provide a continuous pulse train. The output from the timer was passed through a resistor/capacitor values to produce a

sharp negative going pulse which was used to trigger the Schmidt hex invertor, Figure 4.6. The output pulse from the Schmidt trigger was in turn used to trigger two monostables which control:-

a) The total switch off time.
b) The time delay before measurements.

4.11.5 SAMPLE AND HOLD CIRCUIT FOR SID

A third monostable was used to control the time interval needed to sample the SID voltage, and a hold capacitor to store this voltage. With the resistance and capacitor values shown, the total off-time for sampling was established to be 1.4 ms. A polypropylene capacitor (0.047 μF) with the appropriate characteristics of droop rate, acquisition time etc. was selected as the holding device Figure 4.7a and 4.7b.

4.11.6 CHARACTERISTICS OF THE COMPLETE CIRCUIT

As the temperature of the SID changes so the voltage drop across it also changes. The pulse circuit allows this voltage to be monitored and updated with a cycle time of 19.5 milli seconds. The wave forms generated by the various components in the system are illustrated in Figure 4.8. Before applying the technique to an actual electronic package, the pulsing cycle was adjusted so that power was switched on for 97% of the total time, but a facility was provided to vary the mark space ratio Figure 4.7a. Initially this gave rise to cross-talk with the SID voltage, but this was eliminated by introducing two NAND gates Figure 4.9.

4.12 CALIBRATION

Before the SID could be used as a temperature sensor, it was necessary to determine the relation between the voltage drop across it, and its temperature. Two thermocouple were attached to the upper and lower surface of the system board, which was then brought to a known steady-state temperature, in a temperature controlled oven, Figure 4.10a. A -10 V supply and a 10 KΩ resistor was used to forward bias the SID. The calibration curve for a range of temperatures between ambient and 85 °C, is shown in Figure 4.10b. The graph can be seen to be linear, and can be represented by the relation :-

$$T_J = \frac{(V_A - V)}{m} + T_A \qquad (4.5)$$

where:-

T_J = Junction temperature, °C
T_A = Ambient temperature, °C
V = Forward voltage of SID at temperature T, V
V_A = Forward voltage of SID at abient temperature, V
m = Slope of the calibration curve, V/°C

Once the calibration constant m has been determined, the thermal resistance of any test chip can be calculated by substituting the junction temperature evaluated from equation 4.5 into equation 4.1.

When junction temperature measurements are being made on a large number of similar devices mounted on common substrate it is reasonable to expect that the slope

of the calibration curve (the temperature coefficient of the TSP) will be approximately constant for all devices.

To verify this assumption, 10 devices of the same design and construction mounted on a standard PCB were placed in the oven and the 10 temperature coefficients were determined. The relative sample standard deviation of these coefficients was found to be less than ± 3 percent. Thus the above assumption was found to be reasonable.

4.13 MEASUREMENT OF PACKAGE SURFACE TEMPERATURE

Because of the inherent difficulties of attaching a thermocouple to the external surface of the package, and the impractibility of the sputtering process, for most of the experiments surface temperature (T_s) was measured with an infra-red (IR) thermometer. This small, optical, non-contact instrument was focused on a particular point on the surface. Before the quantity of radiation emitted by a surface can be converted to a temperature its emissivity (ε) must be known. To avoid difficulties of estimating emissivity, the small area of the surface on which the instrument was focused was coated with a thin layer of black paint (emissivity near unity).

Finally, as a check, but bearing in mind the difficulties of contact measurements mentioned above, in some experiments, the surface temperature of the package was also measured with a thermocouple.

4.14 TESTING THE COMPLETED SYSTEM

4.14.1 DESCRIPTION OF THE EXPERIMENTAL TEST RIG

The experimental test rig consisted of a custom made PCB and a single DIP package (SN7401) Figure 4.11a. The temperature of the DIP's external leads, PCB, copper tracks and the bottom encapsulant were measured by gluing a lacquer coated thermocouple. To make certain of electrical insulation on the leads and copper tracks, these surface were also coated with lacquer Figure 4.11b.

Each mounted thermocouple was then carefully routed through the PCB to an edge connector, which in turn was connected to a digital thermocouple display unit.

4.14.2 MONITORING TEMPERATURE OF DIP's USING SID AND IR

Two types of logic devices (TTL SN7401 and SN74LS01) were used to test the completed system. The SN74LS01 was chosen in particular because, this device is a low-shut-key device, this means that for the same input power levels it will operate at a lower temperature. To monitor the transient heating condition effectively, the convection from the outside of the packages was reduced by insulating the devices between two pieces of 10 mm polystyrene. The surface and junction temperature of the packages were monitored by means of a conventional thermocouple and a SID respectively. High thermal conductivity paste was used with the surface thermocouple to ensure a good contact. Every minute, for the first five minutes, and then every five minutes for the next ten minutes, the transient temperature of the surface thermocouple

and SID was recorded. Figure 4.12 illustrates the expected low temperature of the SN74LS01 (low shut key) device compared to that of SN7401 when both powered to same levels. This test demonstrated the successful operation of the pulsing board. Figure 4.12 further demonstrated that, the initial transient response of the chip (during the first few seconds of operation) was a steep linear temperature rise. This part of the curve is of a particular importance, because it would decide whether or not it is possible to compare the experimental data with those of the transient theory derived above. To investigate the transient temperature response more accurately when the device is switched on, the DVM was replaced by a x-y chart recorder for subsequent tests.

The test on the SN7401 device was repeated, for different mounting arrangements and heat transfer conditions, as shown in Figure 4.13. The transient temperature response illustrated in Figure 4.13 was normalized with respect to temperature after 30 minutes (steady state condition), Figure 4.14. The analysis of the normalized temperature response illustrates that approximately 80% of the chip temperature rise was reached within the first few seconds of the applying power. This constitute a linear temperature rise when chip is powered up.

Figure 4.15 shows the transient temperature response governed by the exponential form of the theory derived above. Comparison of Figure 4.14 and 4.15 shows that the actual transient response of the chip can not be presented by the simple theory derived above. Since the assumptions made in development of the simple transient theory are not satisfied due to low conductivity of the DIPs plastic body and existence of

temperature gradient on the top surface .

Because of this lack of agreement, it was decided that a more realistic analysis could be achieved by construction of a detailed FE model.

4.15 DETAILED FE MODEL OF DIP (SN7401)

In order to perform a thorough analysis of the test DIP with complex conduction path, (leadframe) a detailed model of DIP was constructed following the leadframe. In this research the details of the internal construction of the TTL SN7401 was obtained by filing away the top encapsulant to revel the leadframe as shown in Figure 4.16. Consideration of symmetry meant that it was necessary to model only 1/4 of the total package.

A three dimensional mesh layout corresponding to Figure 4.16 is illustrated in Figure 4.17, from this figure it can be seen that essentially the model consisted of two parts PCB and DIP. The PCB was constructed of one layer of elements having fine mesh in the vicinity of where leads are connected to PCB. The package (DIP) was constructed of three layers of elements in which the central layer (containing chip, leadframe and tie bar) sandwich between upper and lower slab of plastic Figure 4.18.

In this study a uniform distribution of heat generation within the chip was assumed. This was simulated by setting the internal energy generation (q_i, W/m^3) to a constant value for those elements constituting the chip. Each separate component is modeled

by allocating different material and its appropriate physical properties. The conductivity values used are given in Table 4.1.

Material Description	Thermal Conductivity W/mK	Specific heat capacity J/kgK	Density kg/m^3
package body plastic filled epoxy/polyimid	1.46	1400	1120
lead frame Alloy 42	17.0	385	8930
chip silicon	84.0	702	2328
PCB epoxy	1120	1400	0.9
copper tracks copper	385	385	8930

TABLE 4.1 PHYSICAL PROPERTIES OF MATERIALS.

For typical natural convection test conditions the heat transfer coefficient for the FE model was calculated from equation 3.17 Chapter 3. For air (assuming Pr = 0.707) and substituting for Nusselt and Grashof number equation 3.17 will yield;

$$h = C\left(\frac{T_s - T_a}{x}\right) \tag{4.6}$$

where;

For horizontal surfaces;

x = 2LW (L + W)
C = 1.344 (facing up), 0.672 (facing down)

For vertical surfaces;

x = Vertical height
C = 1.447

For typical test condition the heat transfer coefficient calculated from equation 4.6 has

a value of approximately 7 W/m^2. Calculations which include natural convection and/or radiation require an iterative solution. Figure 4.19 a-b shows a typical steady-state temperature distribution over the external surface of the FE model.

4.16 COMPARISON OF FE MODEL TRANSIENT DATA AND EXPERIMENT

At the inception of this investigation it was considered essential to validate the SID measured temperature with some form of a theoretical analysis. Unfortunately the simple transient theory failed to validate SID measurement. However, FE provided the necessary comparative tool. Comparison of experimental data using SID and IR with FE prediction are shown in Figure 4.20. Although there was good agreement between experiment and theoretical model, predicted temperatures from the FE model were consistently on average 5% higher. This was probably due to inaccuracies in the physical properties of the plastic molding compound, see Table 4.1. Although these values were the best recommendations found after an extensive search of the literature for this type of DIP, they may not be absolutely compatible with SN7401 package.

A further attempt was made to fit the form of equation 4.4 by adopting forced convection as the cooling medium. For forced convection at constant velocity of air, h will be virtually constant. However the results shown in Figure 4.21 demonstrates that a lumped parameter assumption is still not possible due to the temperature gradient that exists within the top surface of the body.

4.16.1 HEATING OF SN7401 TO ITS MAXIMUM OPERATING TEMPERATURE

In normal operating conditions, the current passes through the NAND gates whilst the SID is passive. This test was carried out to establish whether failure of a NAND gate corresponded to a failure of the SID as a TSP. The test device SN7401 was placed in an oven, and the input to one of the NAND gates was maintained at 4 volts whilst the others were pulsed between 0 and 4 volts at a frequency of 7kHz. The output signal of one of the NAND gates was monitored on an oscilloscope.

At about 120°C the amplitude of the output signal decreased from 4 volts to 1 volt. This temperature seemed to bear no relation to the 70°C maximum operating temperature recommended by the manufacturer for this device. However the manufacturer maximum operating temperature may be based on a safety factor. At this point the SID ceased operation, hence proving that the SID is an integral part of the logic circuit, the assumption made during the earlier feasibility study.

4.17 HEAT FLOW ANALYSIS OF 14 PIN DIP USING SID AND FE

Although research of a complex system such as DIP mounted on a PCB, has been carried out by construction of a scaled laboratory model, this usually involves assumptions and limits the accuracy of the results. However, combination of the validated SID (TSP) and detailed FE model, eliminates the need for scale modelling. In this part of the investigation the combination mentioned above was used to analyse

the complex conduction paths and the effect of the PCB on the temperature of the DIP.

In series of tests the DIP (ceramic and plastic) was powered ranging from 23 mW to 100 mW in natural convection both mounted on and off the PCB. The surface temperature was measured with a infra-red thermometer, whilst the junction temperature was monitored by the SID. The leads and copper tracks temperatures were also measured by lacquer coated thermocouples. To compare the FE predictions with experiment, series of FE runs were also carried out simulating the test conditions.

4.17.1 COMPARISON OF MODEL DATA - FE AND EXPERIMENT

Plastic package

Figure 4.22 a-d illustrates the temperature variation along a line from the edge of each lead inside the package (location 1) to a point where each lead is soldered to the PCB (location 3). Location 2 is the point where the lacquer coated thermocouple was attached for experimental measurement, see Figure 4.16. These data revealed the expected uniform temperature distribution within each lead due to its high thermal conductivity. However lead one is shown to be slightly hotter than the other three leads. This is because, lead one has the shortest internal conduction path (approximately 0.5°C). Similarly it is shown that the effect of the PCB is to reduce the temperature of the package on average by 25% hence indicating that the PCB acts as a heat sink.

Ceramic package

For this type of package the general trend in leads temperature was similar to plastic package. However due to high thermal conductivity of the ceramic, the recorded temperatures of each lead is 6% lower than the plastic package. Figure 4.23 a-b illustrate the comparison of the leads temperature between the ceramic and the plastic package with and without PCB.

4.17.2 THE RESISTANCE BETWEEN THE CHIP AND THE LEADS

Figure 4.24a shows the experimental and FE prediction of the temperature variation along a line from the edge of the chip and across to lead one. It should be remarked that from the analysis above the temperature distribution within the leads can be assumed uniform. The data in Figure 4.24a reveal the temperature gradient in the plastic strip which separates leads from chip is approximately 4°C. This gradient does not indicate the presence of a large thermal resistance which might markedly reduce conduction from chip to leads in plastic packages. Since the moulding plastic in DIPs are normally modified with addition of filler, this results in thermal conductivity of the plastic encapsulant being higher than pure plastic. Figure 4.24b illustrates similar analysis with presence of the PCB. As shown the PCB does not effect this resistance as expected.

4.17.3 HEAT FLOW ANALYSIS OF THE DIP

One of the powerful features of the ANSYS FE package is that it allows the heat flow

from all surfaces having a convection to be evaluated. The total convective surface area of the package mounted on a PCB was subdivided in to nine partial surfaces;

1 - Package top, bottom, front and end faces.
2 - 4 leads.
3 - PCB

Analysis of DIP heat flow without PCB

Figure 4.25a illustrates the heat flow through the above mentioned faces for a plastic package. As shown because the heat transfer coefficient is low in natural convection, the temperature distribution is rather even, therefore the percentage heat flow is mainly dependent on the convective surface area. Furthermore, for a plastic package some 29 % of the total energy is transferred from the leads. The low heat transfer from the bottom face (13%) is a consequence of the particularly low h value on this face because it is facing down. Figure 4.25c shows the heat flow effects in moderately higher h value simulating forced convection conditions. The effect of reducing resistance on the outside of the package is to reduce the heat transfer from the leads, this being most marked by lead 4 the furthest from the heat source. The top surface of the package exhibits the highest heat transfer followed by front and then the bottom surfaces. Comparison of the heat transfer from the end face for the two cases investigated is marginal.

Analysis of DIP heat flow with PCB

Figure 4.25 b and d illustrate the percentage heat transfer from all the external surfaces. In natural convection the PCB transfers some 43% of the total energy, indicating that it is an effective heat sink. However, this is reduced to 17% with an increase in h value. This is the direct result of the other faces ability to convect the heat since, they are nearest to the heat source.

4.15 CONCLUSIONS

1) The advantages and disadvantages of various electrical techniques for measuring junction temperature have been investigated and a preferred technique discussed in detail. An electronic circuit was designed and developed to carry out the task of switching and monitoring the substrate isolation diode as a temperature sensitive parameter.

2) The preferred technique, in which the Substrate Isolation Diode is used as temperature sensitive parameter, is usable on most of logic devices. The measuring procedure proved to be relatively simple and the temperature sensitive parameter operates under conditions that simulate normal device operation. Detailed circuit diagrams of the final system have been presented.

3) A calibration procedure was described and a simplified procedure to extend the technique to a production environment was validated. The system was then applied to commercial DIP's and scarce transient data have been presented.

4) The FEM has been used to construct a realistic detailed theoretical model of 14 pin dual-in-line package. Transient FE runs were also compared with the SID transient measurements.

5) The maximum operating temperature recommended by manufacturers was exceeded during device failure test, proving the SID to be an integral part of the chip.

5) The technique has been used to carry out detailed analysis of the conduction path in DIP. Comparison was also made to a similar package in ceramic substrate. the technique also enables accurate evaluation of the thermal resistance of the package.

6) The manner in which the heat transferred from the plastic package is distributed over external surfaces was determined.

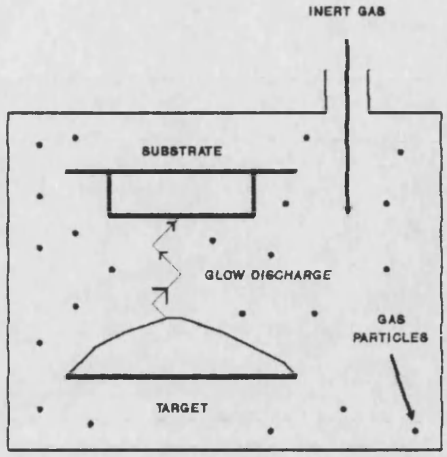


FIGURE 4.1a - SPUTTERING VACUUM CHAMBER

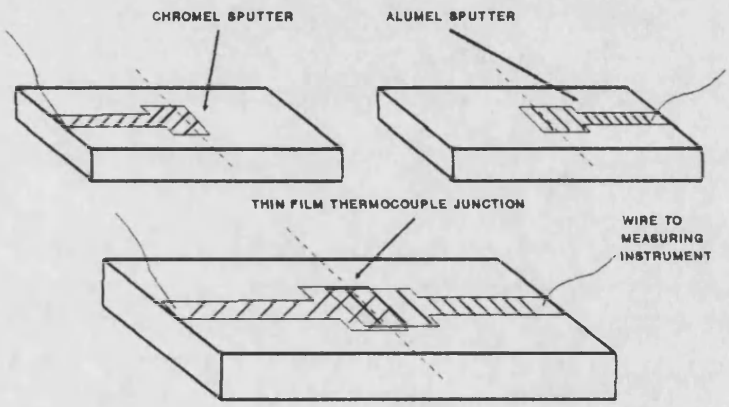


FIGURE 4.1b - SPUTTERING A DIP

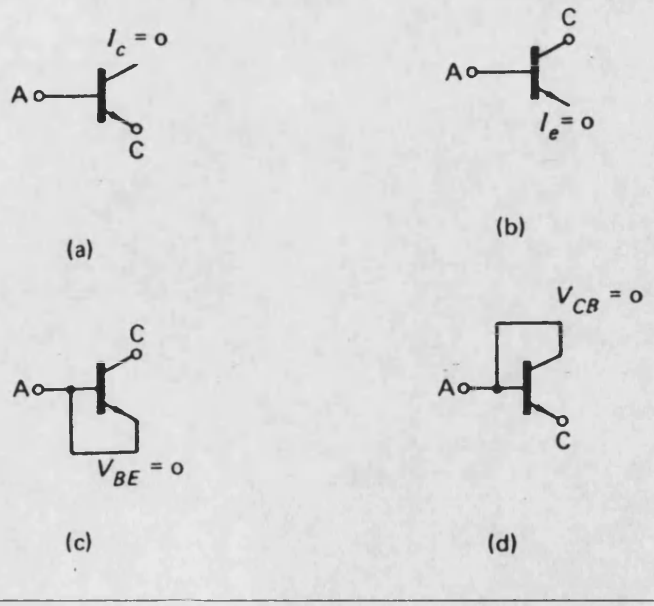


FIGURE 4.2 - POSSIBLE CONNECTIONS FOR AN INTEGRATED DIODE

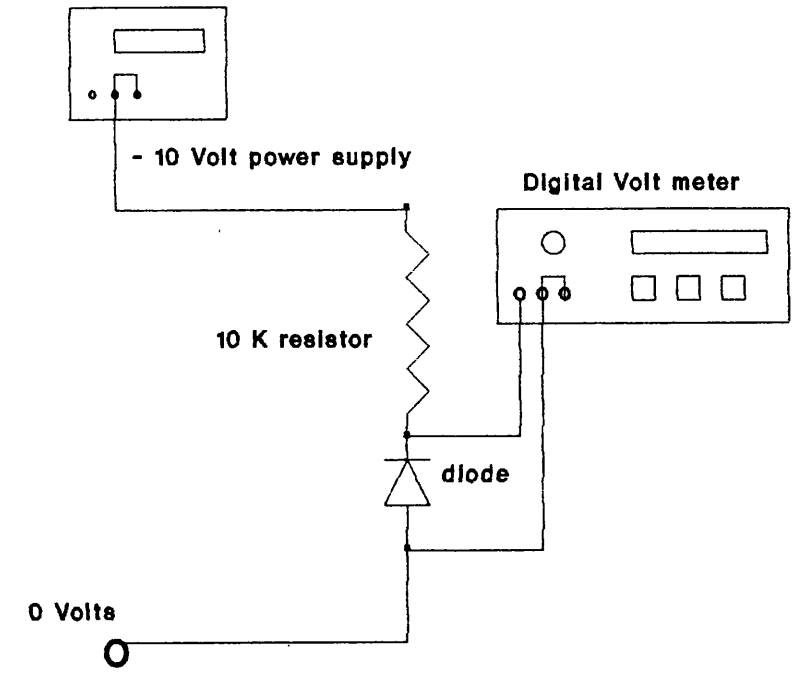
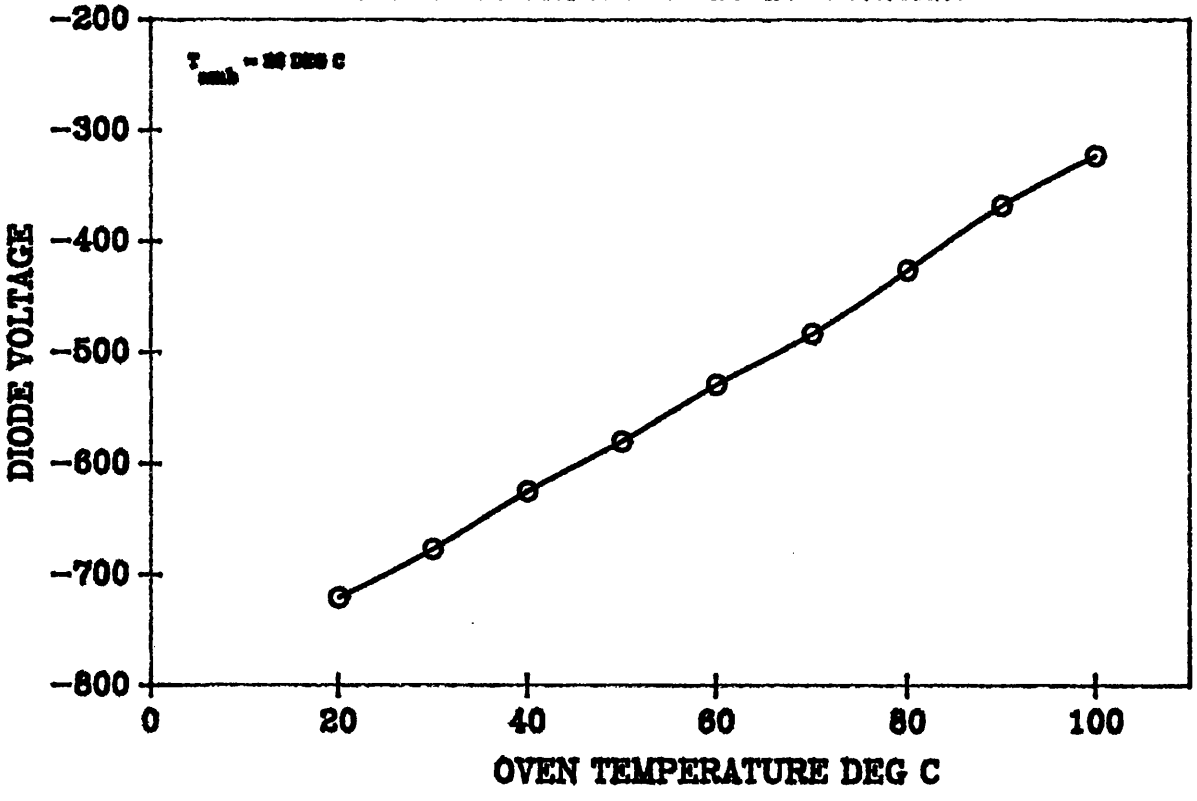
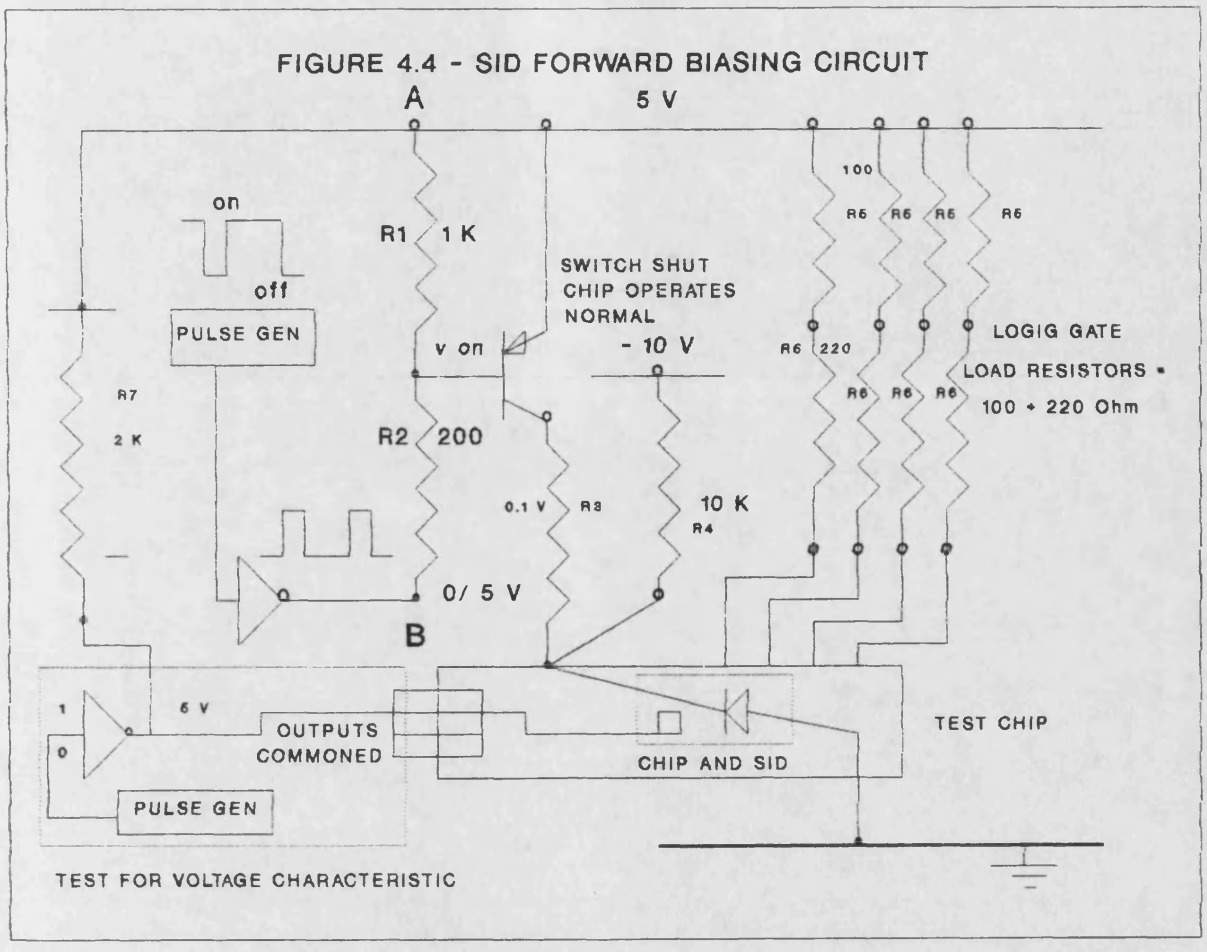


FIGURE 4.3a - MONITORING THE CHARACTERISTICS OF THE DIODE

FIGURE 4.3b

CHARACTERISTIC OF DIODE WITH INCREASING TEMPERATUR





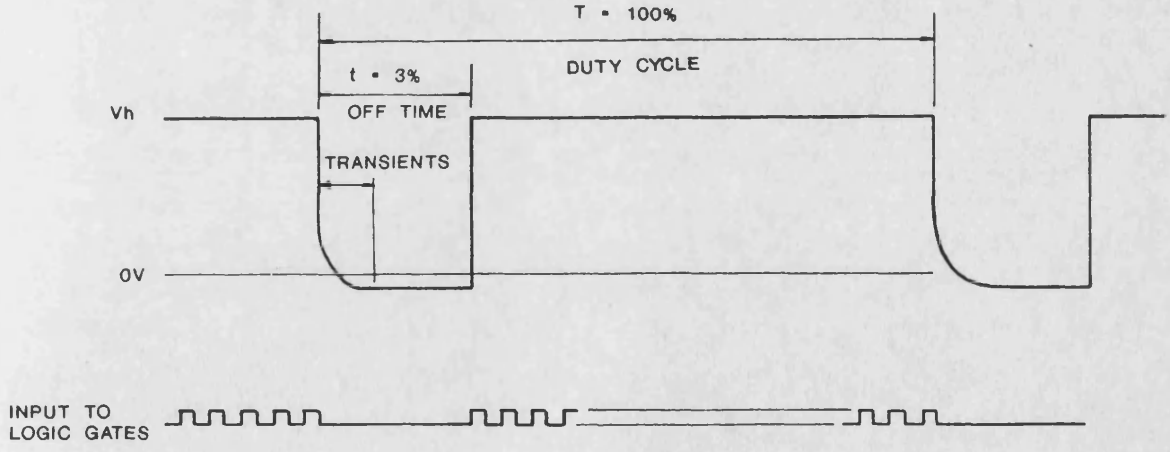


FIGURE 4.5 - TOTAL OFF TIME OF INPUT SIGNAL AND TRANSIENT EFFECTS OF INPUT VOLTAGE

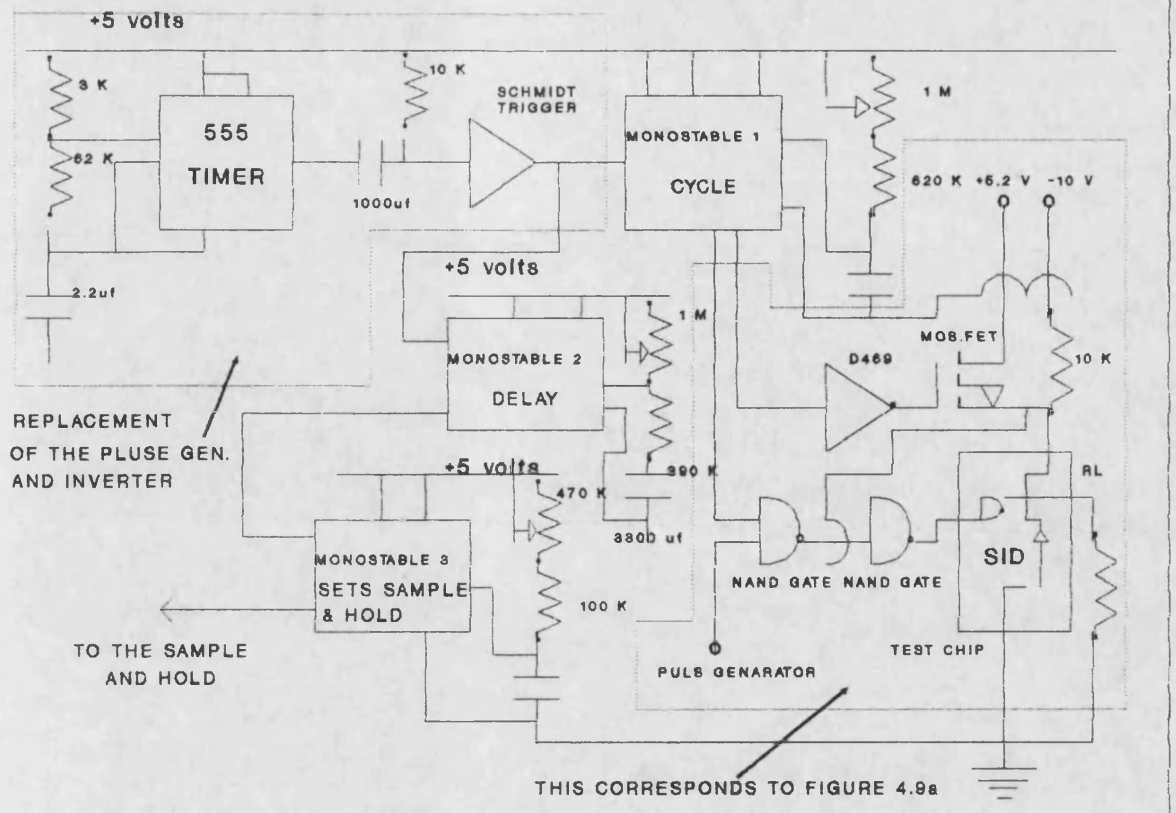


FIGURE 4.6- AUTOMATIC TIMING OF THE PULSING BOARD

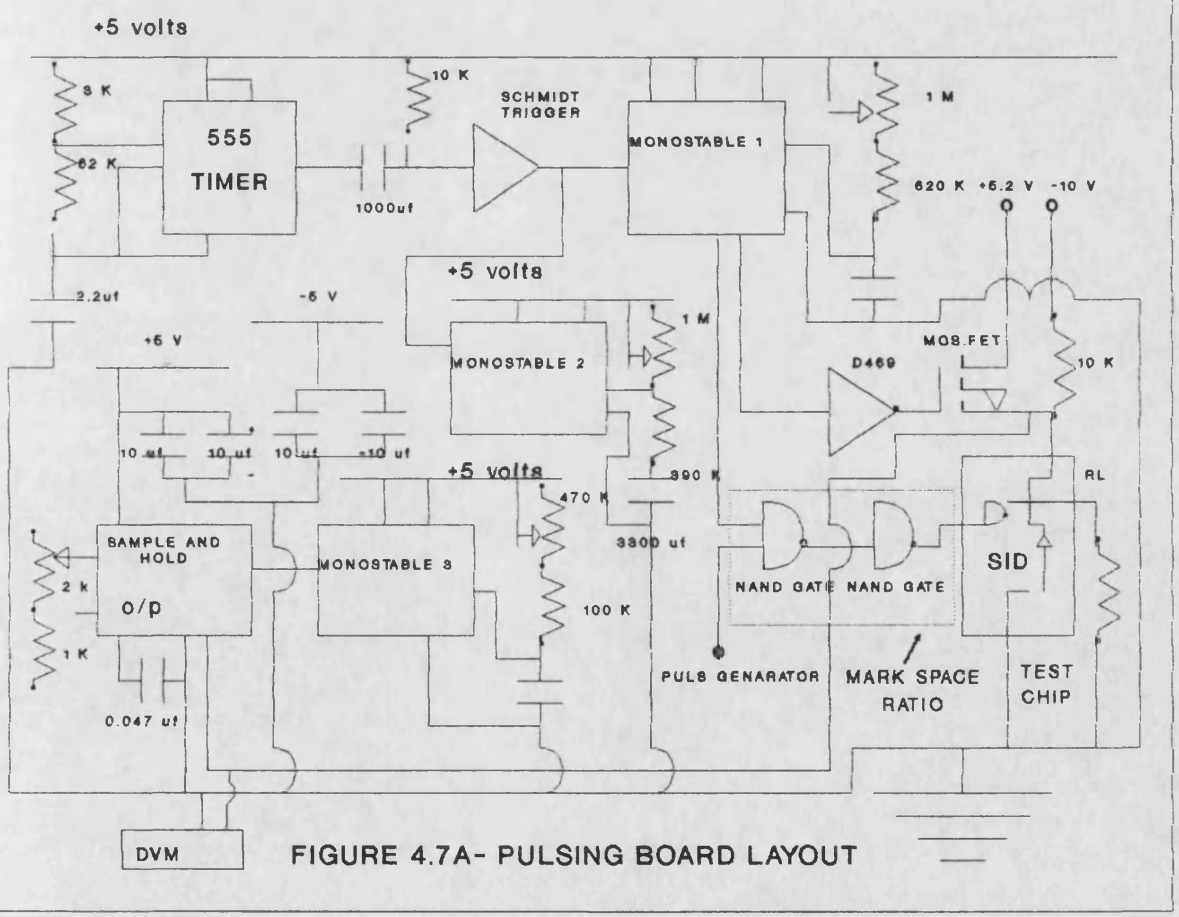


FIGURE 4.7A- PULSING BOARD LAYOUT

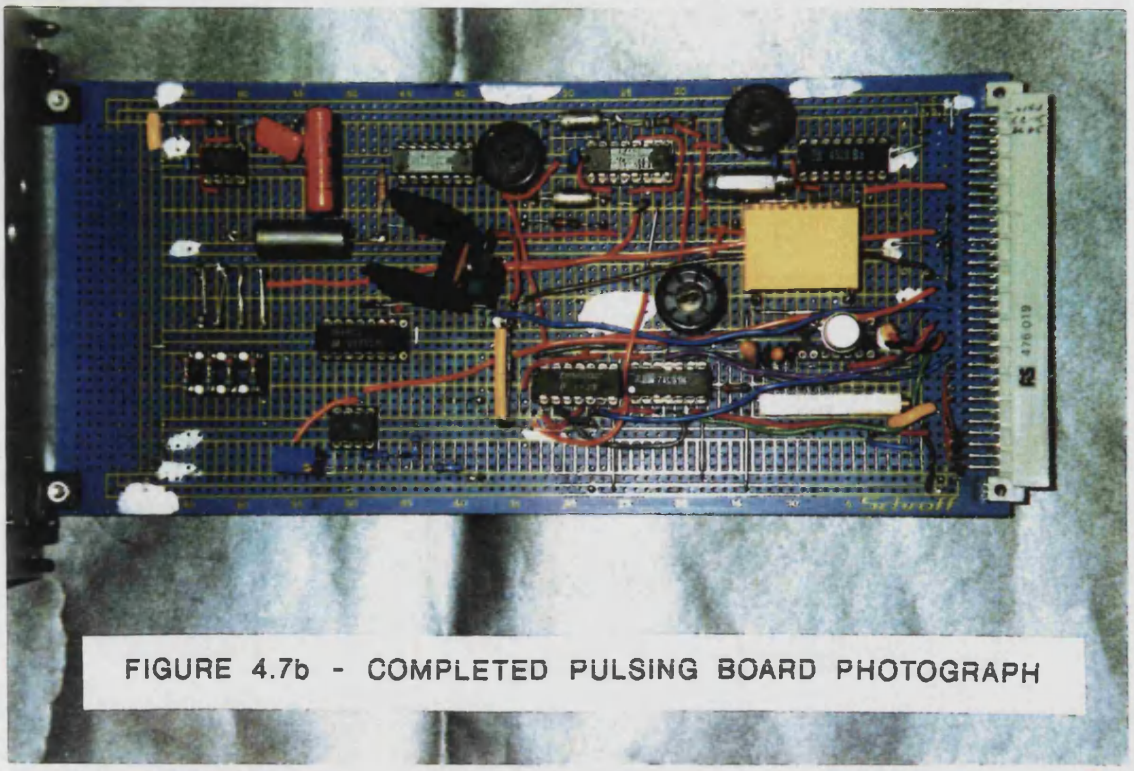


FIGURE 4.7b - COMPLETED PULSING BOARD PHOTOGRAPH

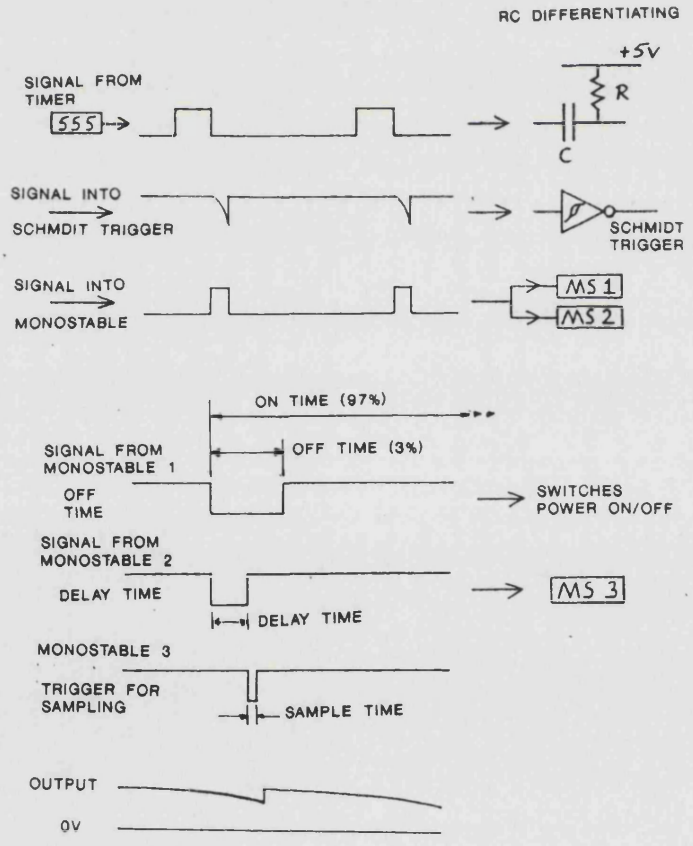


FIGURE 4.8 - PROGRESSION OF WAVE FORMS THROUGH THE PULSING BOARD

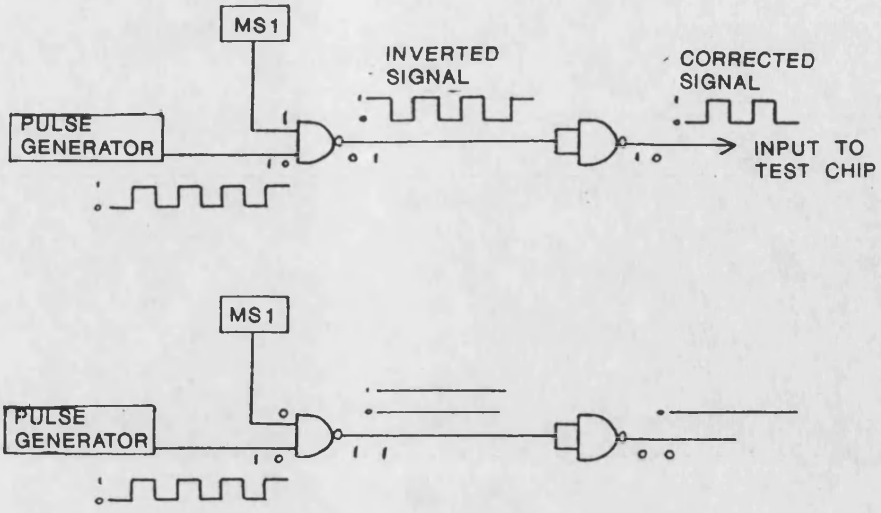


FIGURE 4.9 - ELIMINATION OF CROSS TALK

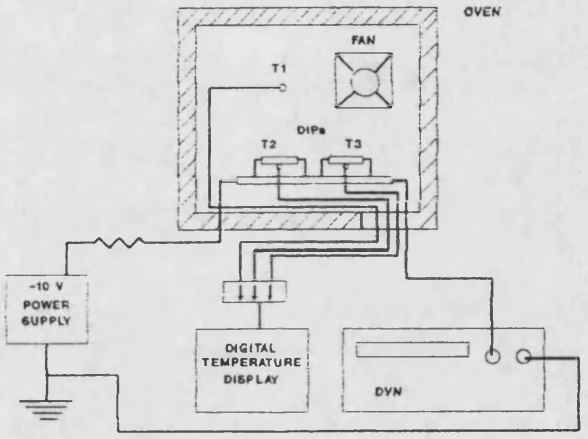
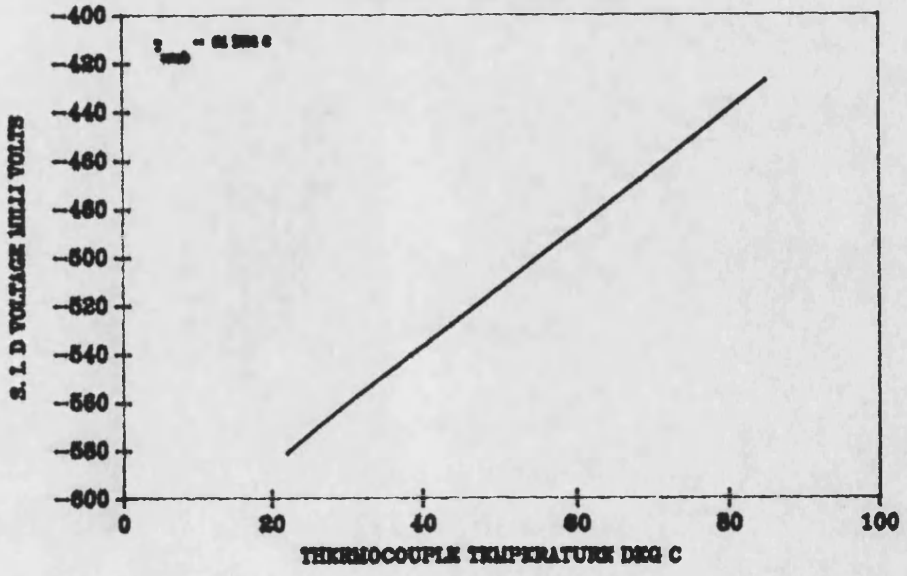


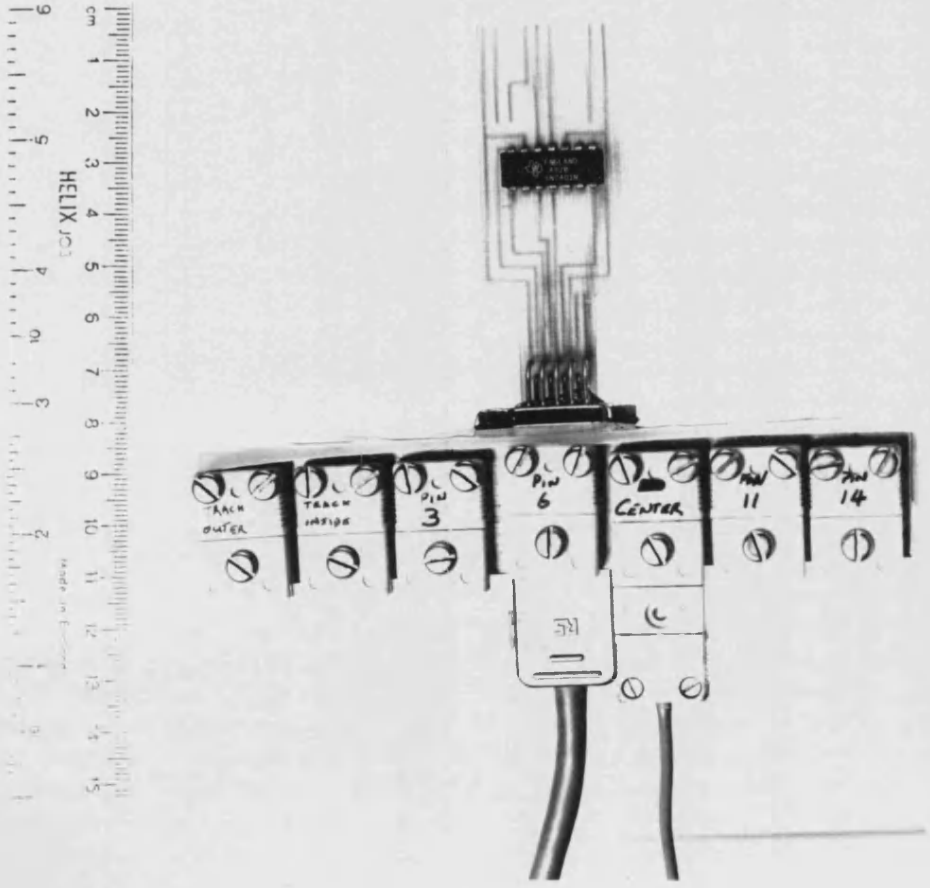
FIGURE 4.10a - DIP CALIBRATION SET UP

FIGURE 4.10b

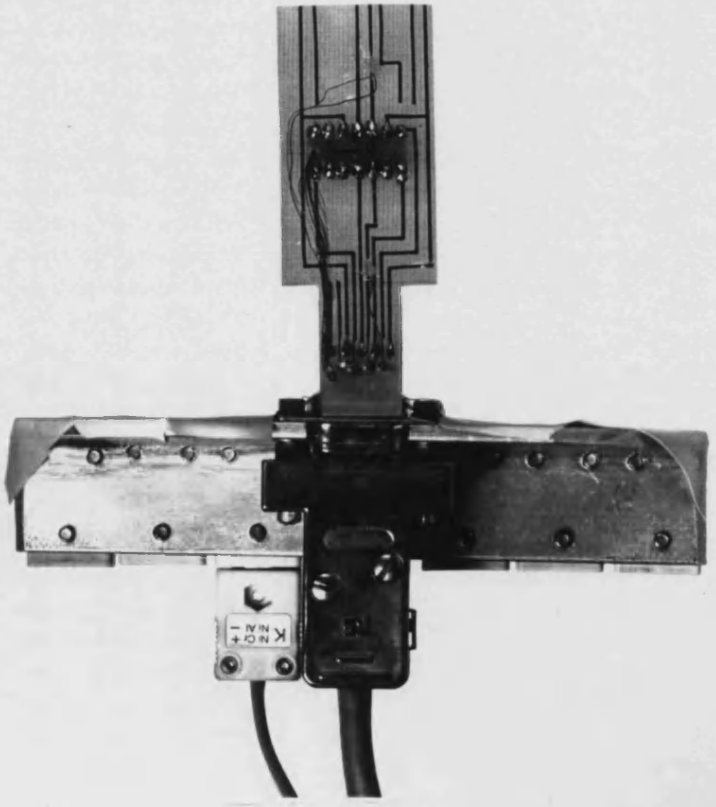
CALIBRATION CURVE SID VOLTAGE vs TEMPERATURE FOR TTL 7401 TEST CHIP



4.11a - TOP VIEW



4.11b - UNDER SURFACE VIEW



TEMERATURE MEASUREMENT TEST RIG -
DIP (SN7401) MOUNTED ON PCB (SID,LEADS AND COPPER TRACKS)

FIGURE 4.12
TRANSIENT RESPONSE OF THE CHIP AND PACKAGE SURFACE
DEVICE MOUNTED ON PCB AND INSULATED

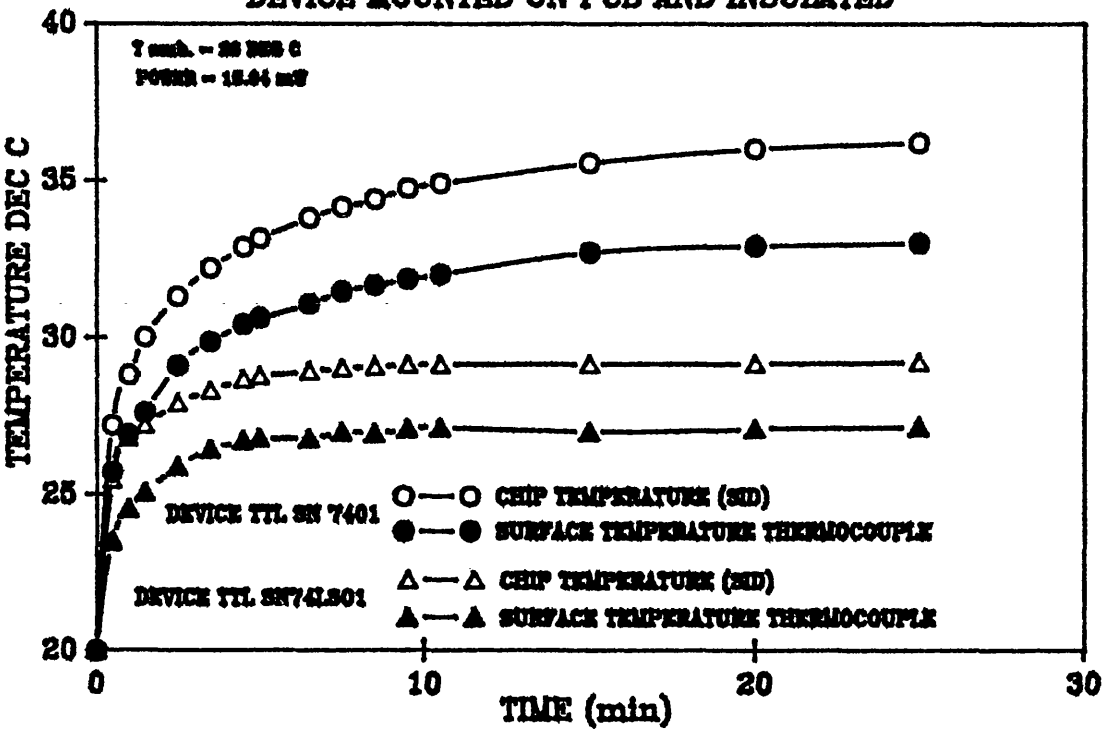


FIGURE 4.13
TRANSIANT TEMPERATURE RESPONSE OF THE CHIP WITH VARYING
HEAT TRANSFER AND MOUNTING CONDITIONS

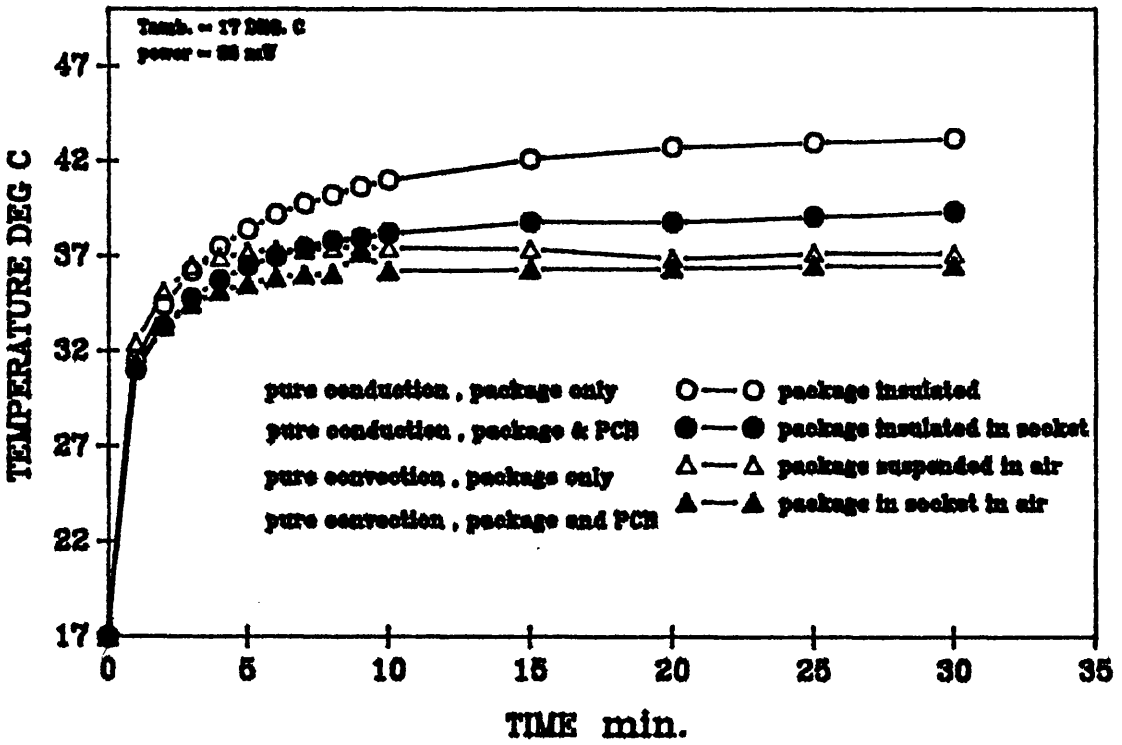


FIGURE 4.14
NORMALIZED TEMPERATURE VERSUS TIME PACKAGE TRANSIENT RESPONSE

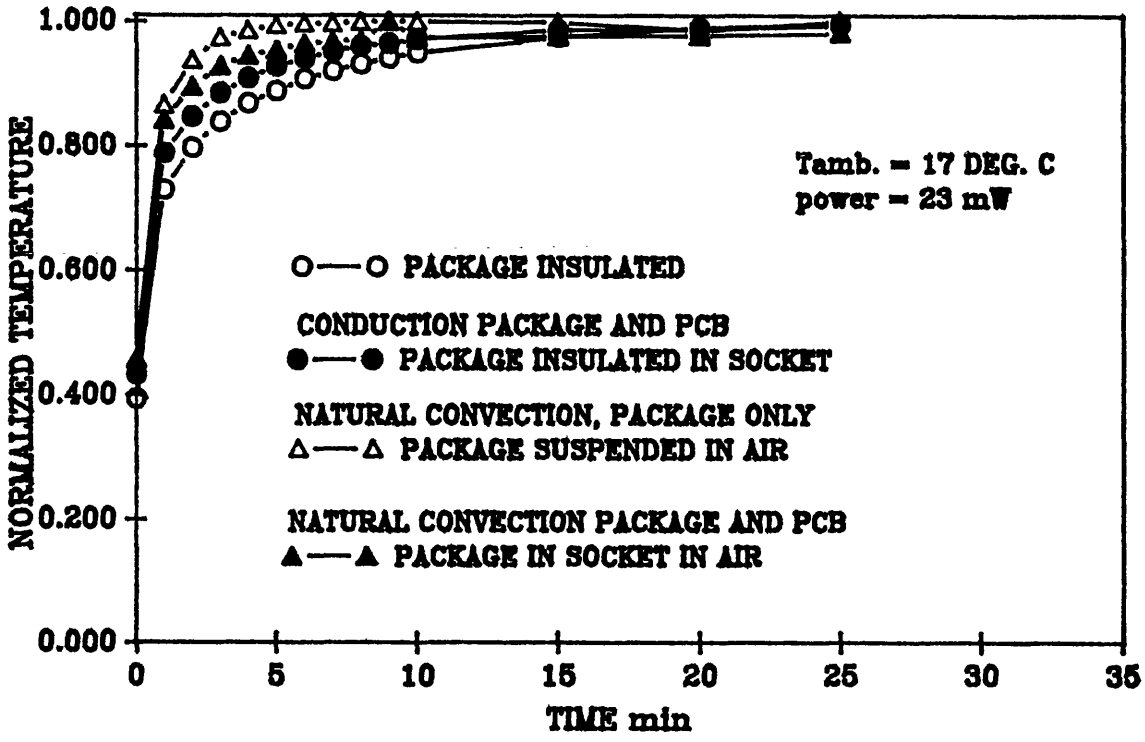
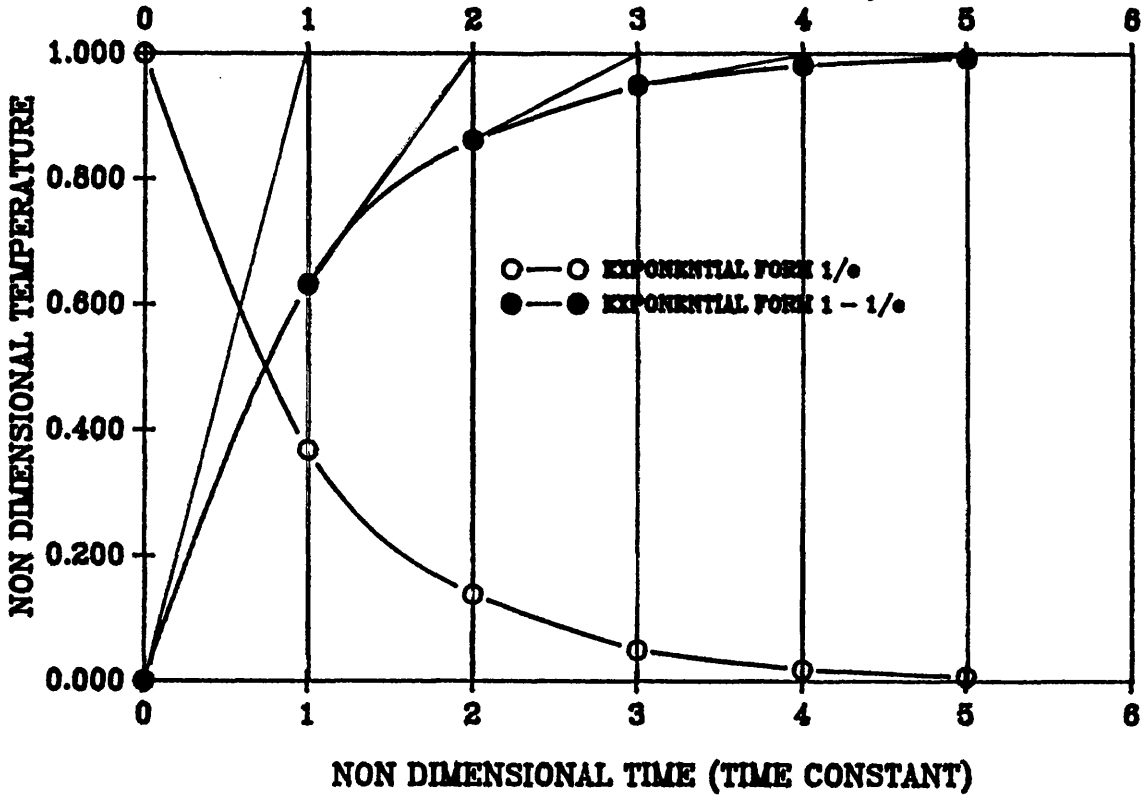
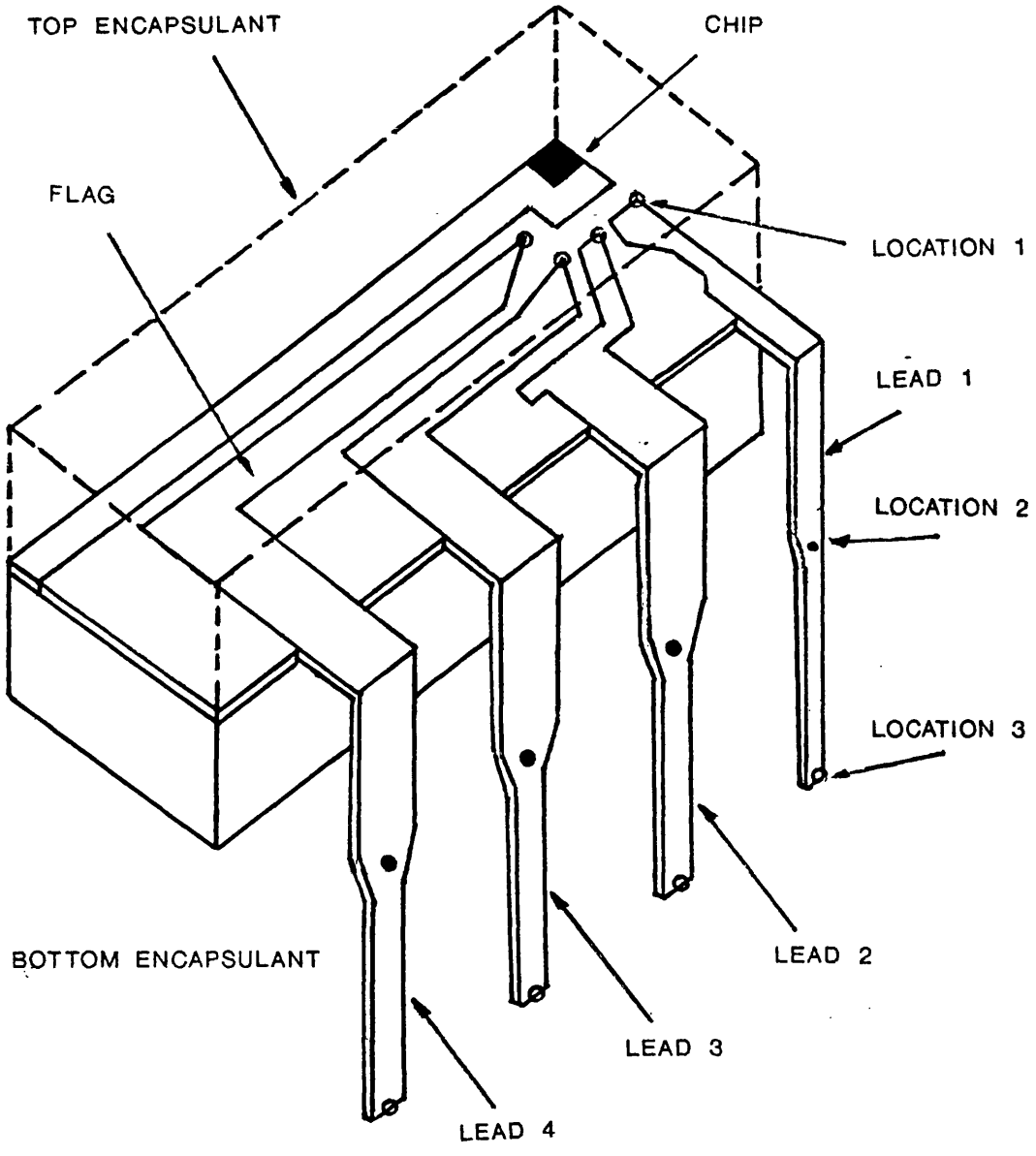
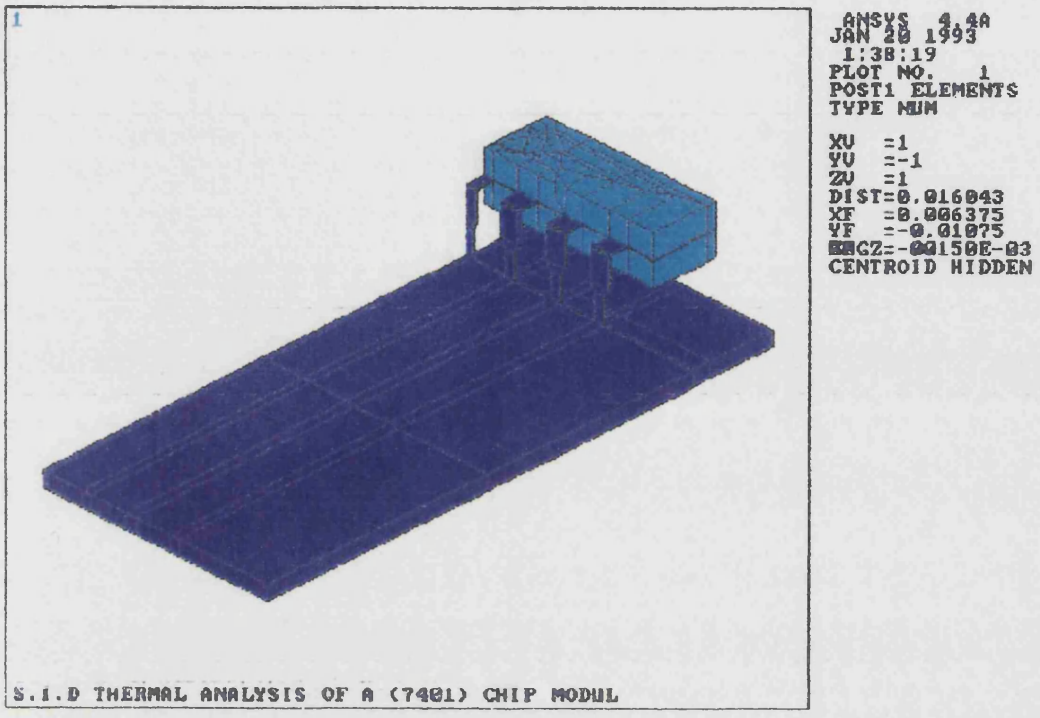


FIGURE 4.15
CONSTUCTION OF A EXPONENTIAL CURVR EQUATION 4.3

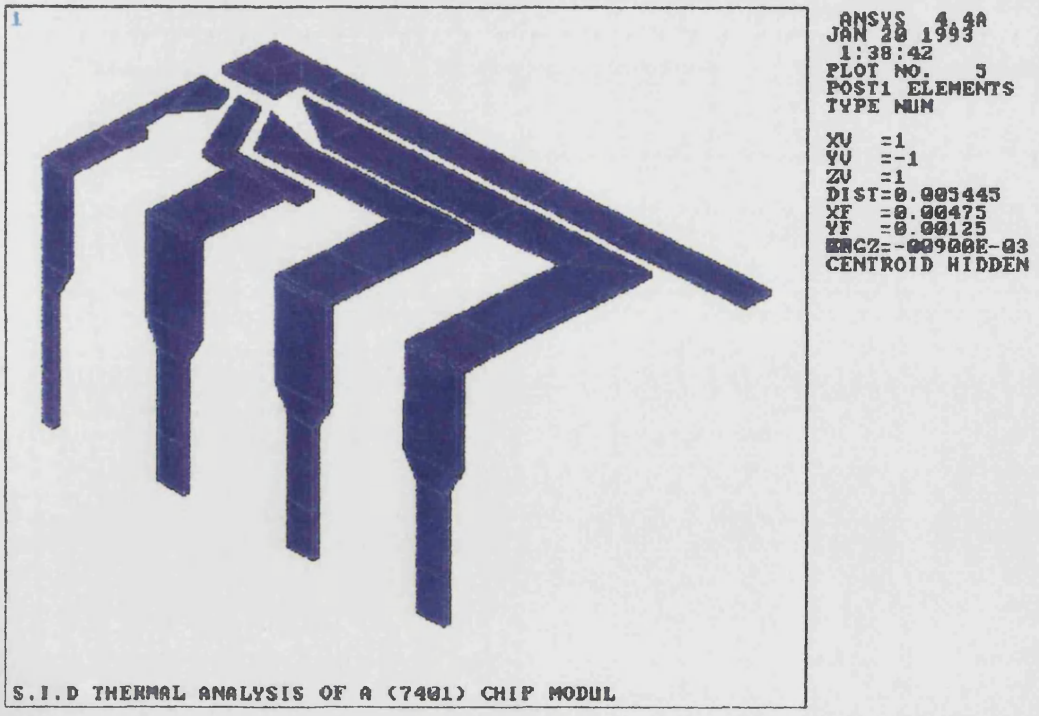




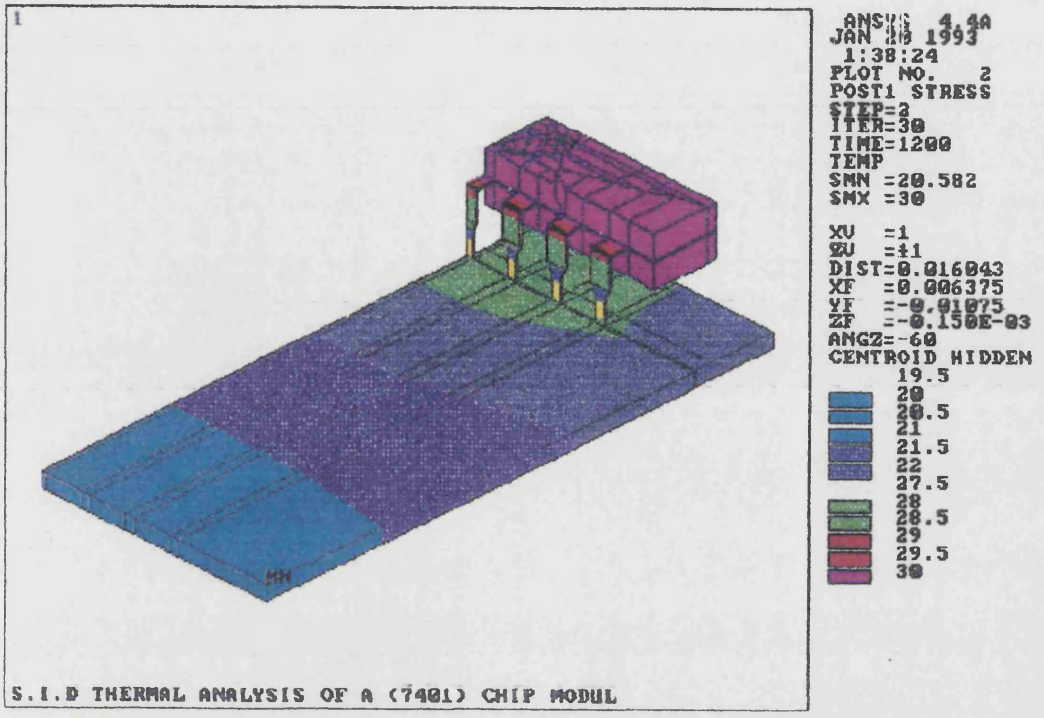
4.16 - INTERNAL CONSTRUCTION OF DIP (TTL SN7401)



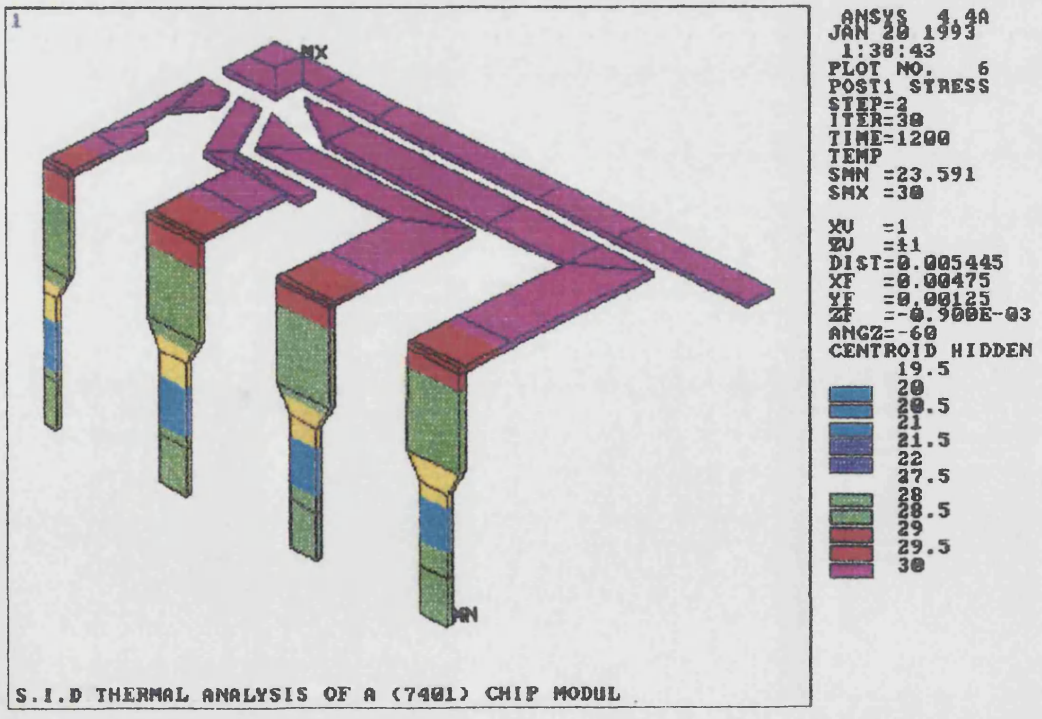
4.17 - FINITE ELEMENT MODEL OF TTL SN7401 DIP



4.18 - LEAD FRAME MESH CONSTRUCTION



4.19a - TYPICAL TEMPERATURE DISTRIBUTION OF DIP
(H = 5 W/m**2K)



4.19b - TYPICAL TEMPERATURE DISTRIBUTION IN THE LEAD FRAME
(H = 5 W/m**2K)

FIGURE 4.20

EXPERIMENTAL AND FE PREDICTED TRANSIENT TEMPERATURE RESPONCE OF DIP MOUNTED ON PCB IN FORCED CONVECTION

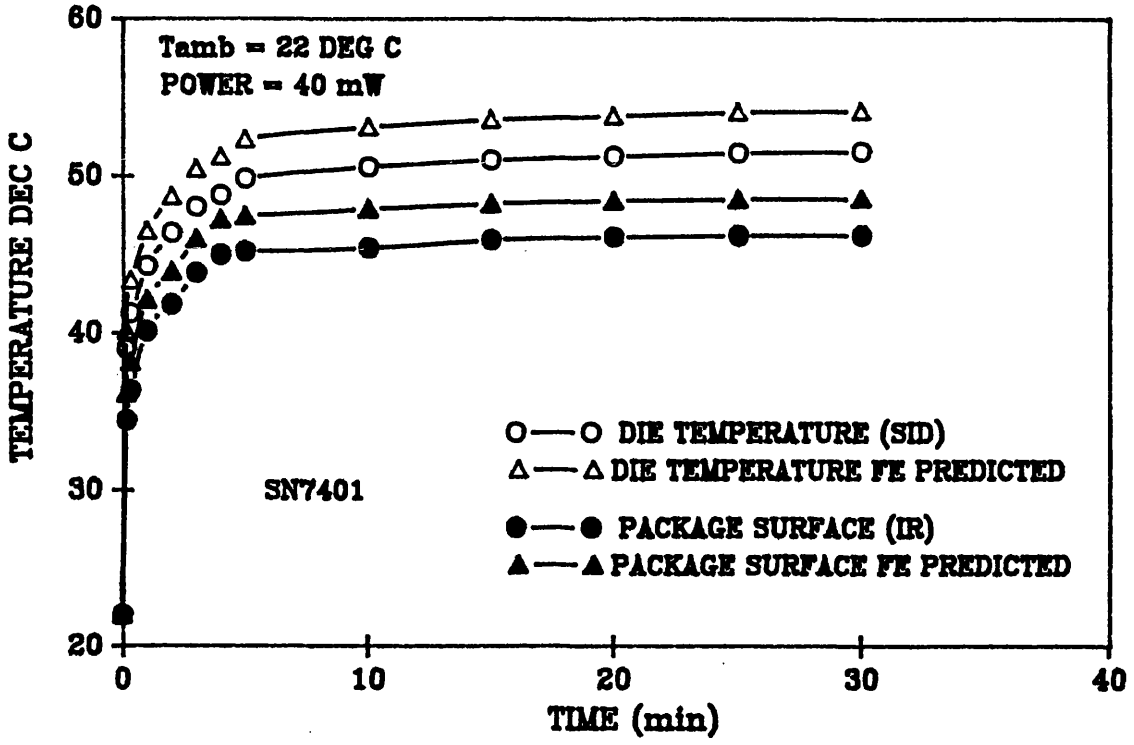


FIGURE 4.21

FE PREDICTED TEMPERATURE DISTRIBUTION ACORSS THE DIP SURFACE IN FORCED CONVECTION

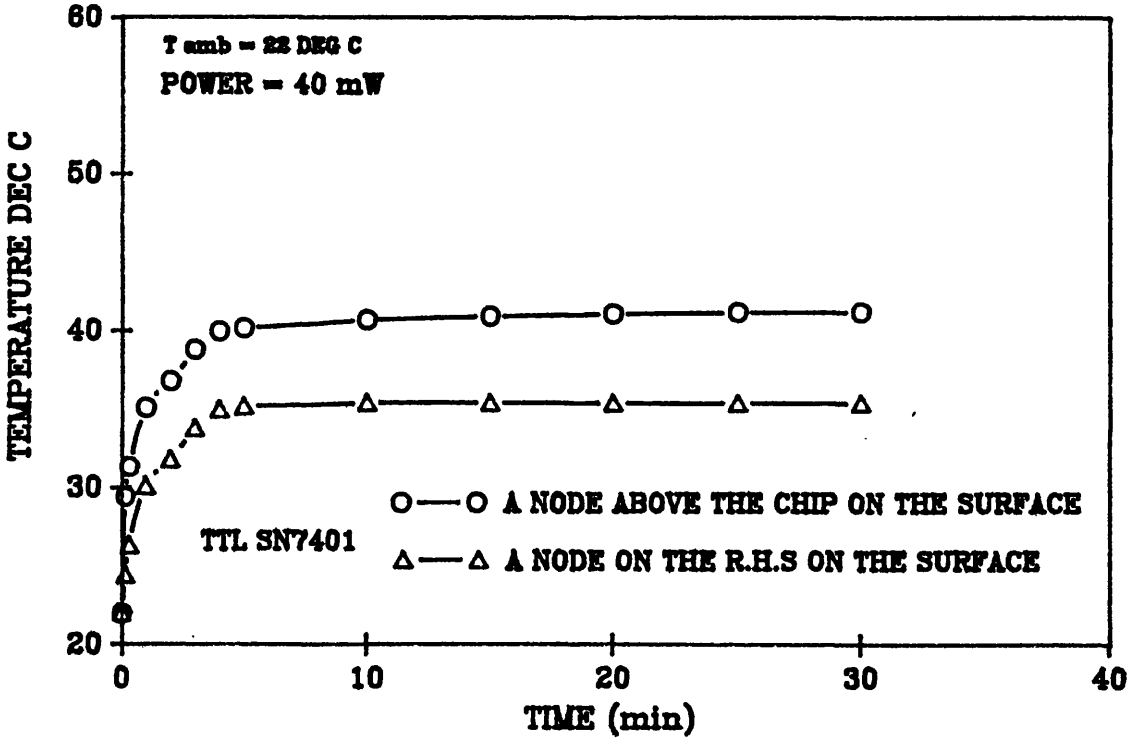


FIGURE 4.22a - (PLASTIC SN7401)
TEMPERATURE vs LOCATION
WITH AND WITHOUT BOARD

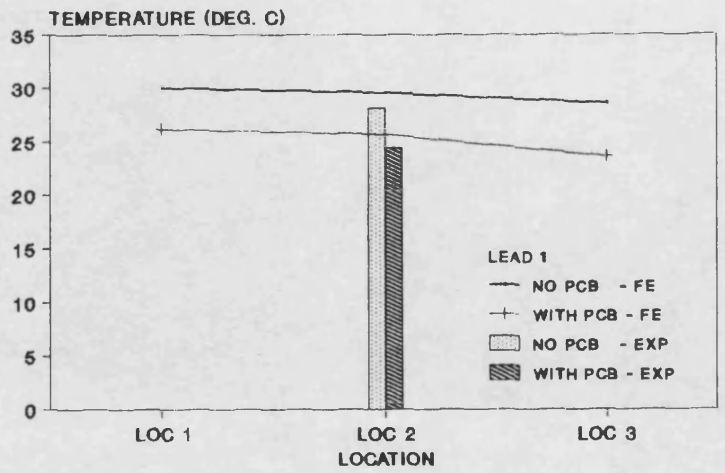


FIGURE 4.22b - (PLASTIC SN7401)
TEMPERATURE vs LOCATION
WITH AND WITHOUT BOARD

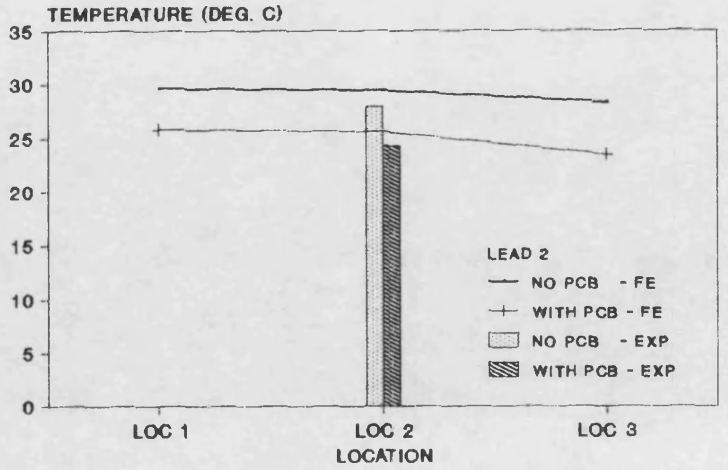


FIGURE 4.22c - (PLASTIC SN7401)
TEMPERATURE vs LOCATION
WITH AND WITHOUT BOARD

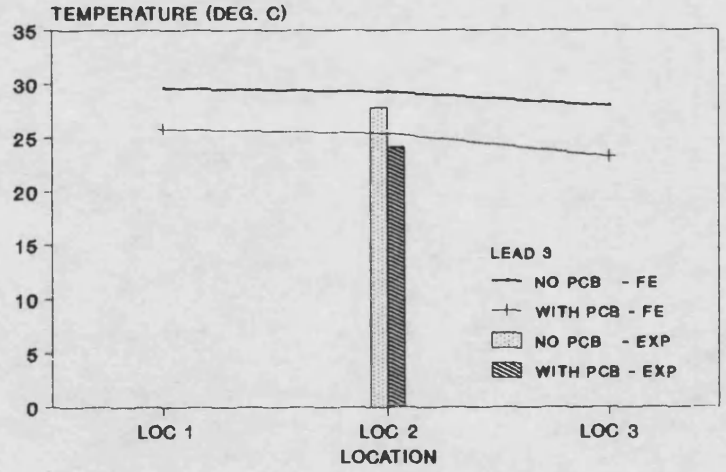


FIGURE 4.22d - (PLASTIC SN7401)
TEMPERATURE vs LOCATION
WITH AND WITHOUT BOARD

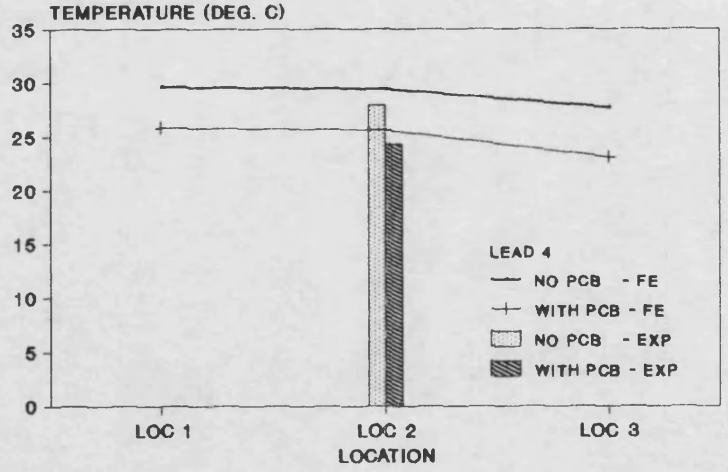


FIGURE 4.23a -(PLASTIC SN7401 & CERAMIC)
TEMPERATURE vs LOCATION
WITH AND WITHOUT BOARD

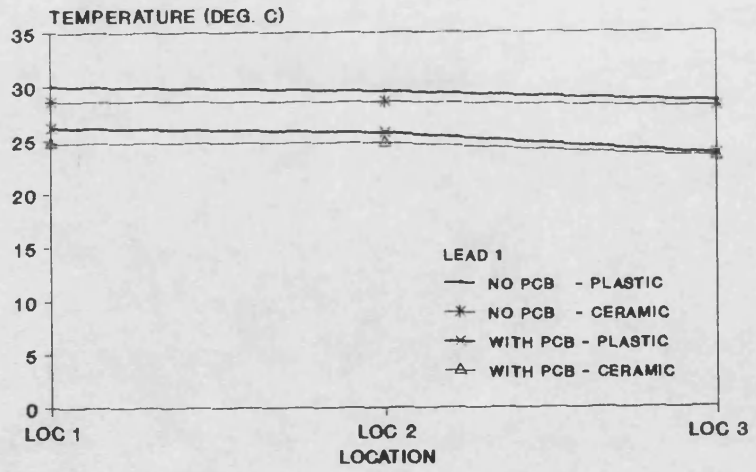


FIGURE 4.23b -(PLASTIC SN7401 & CERAMIC)
TEMPERATURE vs LOCATION
WITH AND WITHOUT BOARD

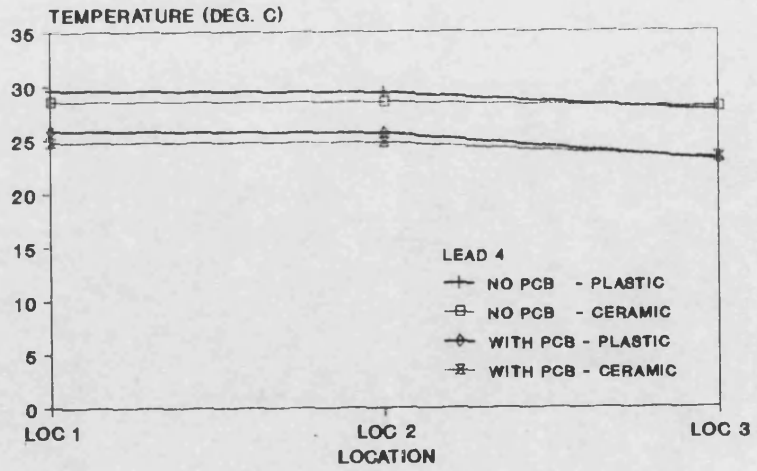


FIGURE 4.24a - (PLASTIC SN7401)
TEMPERATURE vs LOCATION
WITHOUT BOARD (FE & EXPERIMENT)

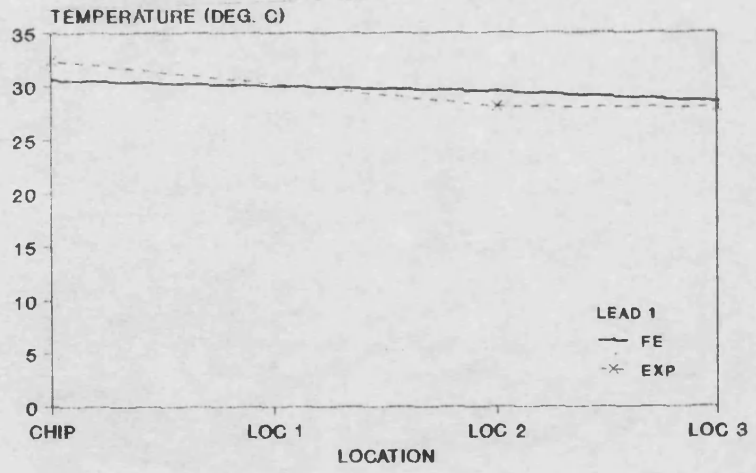


FIGURE 4.24b - (PLASTIC SN7401)
TEMPERATURE vs LOCATION
WITH BOARD (FE & EXPERIMENT)

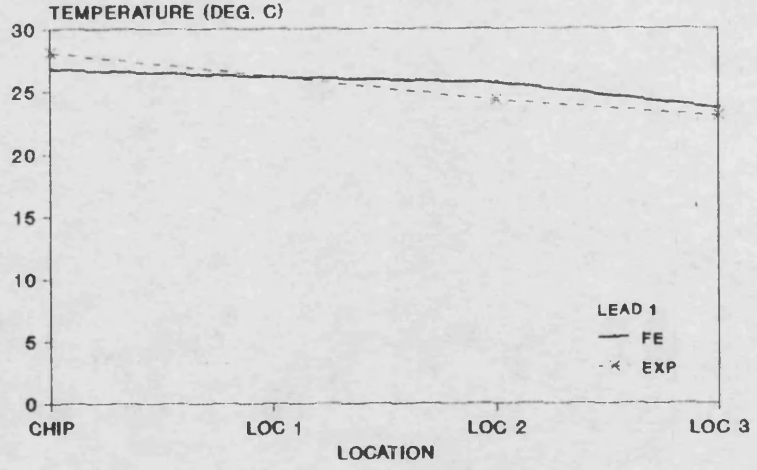


FIGURE 4.25a - PLASTIC
PERCENTAGE HEAT FLOW DISTRIBUTION IN DIP
(WITHOUT PCB) (HCOF = 5 W/m-2)**

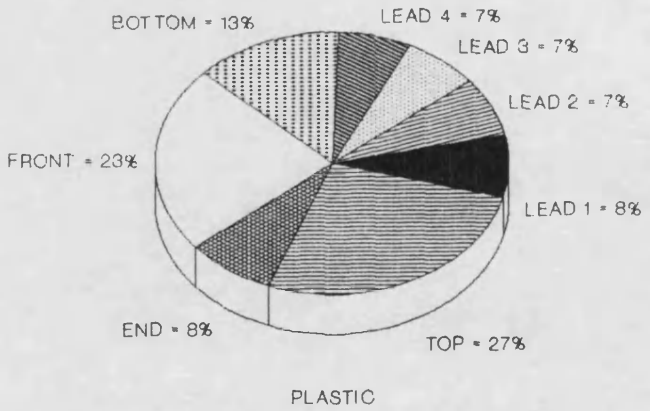


FIGURE 4.25b - PLASTIC
PERCENTAGE HEAT FLOW DISTRIBUTION IN DIP
(WITH PCB) (HCOF = 5 W/m-2)**

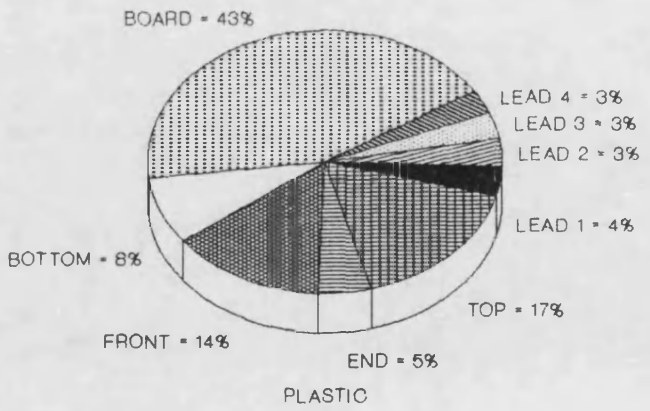


FIGURE 4.25c - PLASTIC
PERCENTAGE HEAT FLOW DISTRIBUTION IN DIP
(WITHOUT PCB) (HCOF =25 W/m-2)**

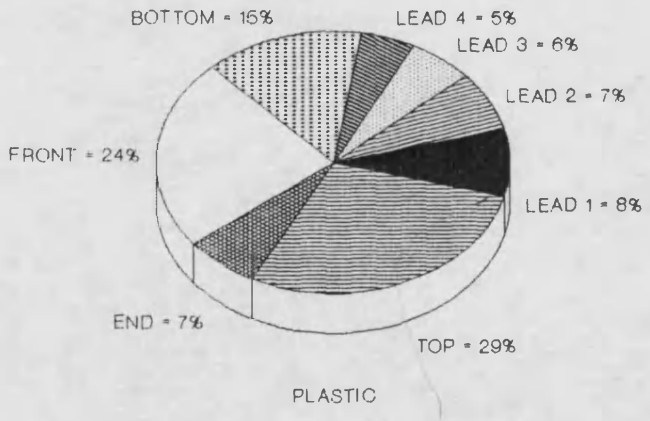
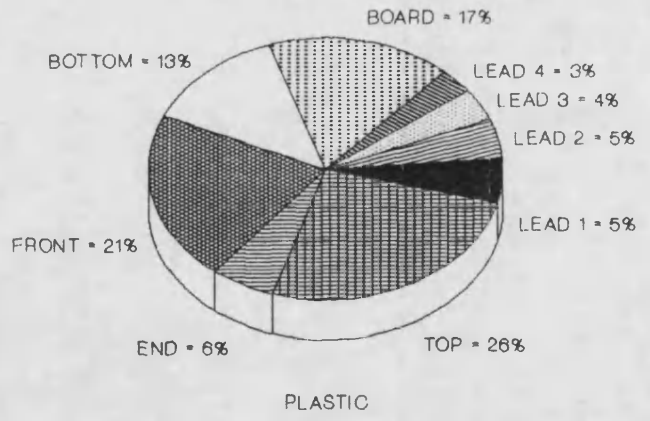


FIGURE 4.25d - PLASTIC
PERCENTAGE HEAT FLOW DISTRIBUTION IN DIP
(WITH PCB) (HCOF = 25 W/m-2)**



CHAPTER 5

THERMAL INVESTIGATION OF CHIPRACK MODERN-ELECTRONIC PACKAGING SYSTEM

5.1 INTRODUCTION

A Chiprack is an interconnection system aimed at removing the constraints generally experienced in standard 2D printed circuit board and associated connector designs. It is capable of supporting both simple and three dimensional interconnections between circuit "blocks" by stacking up its own type of component carrier. The system consists of two main elements:-

1) Component carrier.
2) Connectors.

The carrier holds VLSI circuits in either die or in a surface mount package form. They are double sided and have contact pads on both upper and lower surfaces.

The chiprack connectors join the upper surface of one carrier to the lower surface of the adjacent carrier, in rack or stacked format. In turn the stack is bolted to a motherboard containing signal buffer. Because all of the signals are present at the outside of the stack Figure 5.1, they are easily accessible for test and interconnection purposes. The shape of the connector is not fixed and can be adapted to suit a particular application Figure 5.1 and 5.2.

Another obvious advantage of the chiprack system is the cost effective assembly, since

mass produced connectors and carriers are used. It is also efficient in terms of space saved. One small prototype system based around the Z80 processor, mounted on a chiprack by Dowty Electronics, is estimated to occupy 20% of the volume required to implement the same design in conventional DIPs.

5.2 DOWTY CHIPRACK

A prototype chiprack system designed by DOWTY was presented to the author's supervisor at Bath University for thermal analysis. The chiprack consists of the following four main elements as shown in Figure 1.12a;

i) The semiconductor - An unencapsulated die, bonded to the surface of the chip carrier.

ii) The chip carrier - To support the chip and to allow correct signal routing.

iii) The chip cover - To protect the chip from the environment.

iv) The connector - To support the chip carrier and provide means of transmitting signals, between the adjacent levels of the stack.

The thermal analysis of a chiprack system would require a non-contact method of temperature measurement, because the chip carrier is unencapsulated and protected from environment by a removable chip cover. The chip cover is simply a piece of plastic placed directly above the chip and is not in contact with the chip.

Due to the rack system, the use of infra-red techniques as a method of temperature measurement is impossible, since the line of sight only exists to the uppermost level. It was thought that the method of temperature measurement described in chapter 4,

(SID) was particularly suitable for thermal investigation of the chiprack system.

5.3 OBJECTIVES

The objectives of this investigation was to analyze the pattern of heat transfer in the stack, and to suggest possible methods of cooling. The analysis was as follows:-

1) To carry out experimental investigation of the chiprack system using the SID temperature measurement method (chapter 4).

2) To complement the experimental data with a fully 3D finite element model, and to investigate the temperature distribution within the chiprack stack system using the FEM.

5.4 THERMAL PROBLEMS ASSOCIATED WITH THE CHIPRACK

In solving a microelectronic packaging problem, however, the chiprack creates its own heat transfer problems. The heat generated by the semiconductors may not be adequately dissipated and can lead to a substantial rise in the temperature of the stack. To prevent thermal failure, the semiconductors must be kept below a critical temperature.

5.4.1 CONFIGURATION OF THE CHIPRACK UNDER INVESTIGATION

The Chiprack used in this part of the research was composed of four levels, each containing a single TTL 7400 unencapsulated chip, bounded to a surface of the chip carrier as shown in Figures 1.12a and 1.12b. The rack was placed in a spacer which served to transmit the signal up and down to the other levels. Four of these spacers,

with associated chip and chip carriers, formed the complete system when bolted to the motherboard.

5.5 FINITE-ELEMENT ANALYSIS

In order to construct a 3-D finite-element model of the chip carrier, the research version of the widely used commercial ANSYS package was used. The model was kept as simple as possible. Copper tracks were simulated by having a thin layer of elements on the top and bottom of the chip-carrier which were originally defined to be the same material as the carrier itself, but could be changed to represent the copper tracks if necessary. These tracks were never used.

It was possible to model only one eighth of the chip-carrier due to symmetry. However, on single level analysis, one quarter reduced, provided a clearer visualisation of the chiprack model. When modelling all four levels of the chip-carrier, it was necessary to use the full one eighth reduction. This was required to keep in line with the wave-front and virtual memory limitations as well as reducing the time taken to run the model. The power input to the chip was given in the form of an internal heat generation W/m^3 and the accuracy of the model therefore, was not affected by modelling only a fraction of the chip.

It was expected that the maximum temperature will occur at the chip, and the minimum occurring at the edge of the chip-carrier. This was reflected in the way that the mesh density was very high at the centre of the carrier, but dropping towards the

edge, giving very large elements.

5.5.1 BOUNDARY CONDITIONS

The boundary conditions of the FE model was programmed in an ANSYS user file automatically indexing the following:-

1) Heat generation rate per unit volume of the chip element, to each level or combination of any level.

2) Surface heat transfer coefficient was applied to the exposed surfaces of mother board and stack.

The values of the thermal conductivity used in the model are given in Table 5.1.

No.	MATERIAL	CONDUCTIVITY
1	CHIP/SILICON	147
2	CHIP COVER/PLASTIC	0.20
3	CHIP CARRIER/EPOXY	0.31
4	COPPER TRACKS	390
5	AIR	0.026

Table 5.1 - THERMAL CONDUCTIVITIES OF MODELLED MATERIALS (W/mK).

5.5.2 SINGLE LEVEL FINITE ELEMENT MODEL

A simple, one-level model was constructed first. In this model convection was only applied to the vertical sides of the rack system. The top and bottom horizontal faces were assumed adiabatic. This was to simulate an infinite stack system, where the surfaces receive equal amount of heat as they loose. This model should therefore simulate the second or third levels in the stack. Horizontal and vertical mesh views are illustrated in Figures 5.3 and 5.4 respectively.

5.5.3 THE ONE EIGHTH MODEL OF THE WHOLE STACK

In order to obtain a more accurate map of the heat flow path in the stack, the single level model was replicated four times to model all four levels on the mother board. However, because of the large number of elements involved in the one quarter model, this was divided along the remaining line of symmetry. The resulting one-eighth simulation of the complete stack is shown in Figures 5.5 and 5.6. In addition to this, the two thin layers of elements on either-side of the chip-carrier available to model the copper tracks were removed. The FE runs of the single level proved that these elements were not necessary.

The motherboard was modelled as one layer of elements with convection applied to the exposed area. Convection was also applied to the top surface of the uppermost level, including the surface of the chip cover and vertical sides of the stack.

5.5.4 VALIDATION OF THE FE MODEL

Validation of the finite-element model was carried out by using the following methods;

a) Checking the value of the heat transfer coefficient applied to the vertical and horizontal surfaces of the model against the natural convection theory.

b) Verify the self consistency of the FE model by plotting the variation in the chip, chip carrier and plastic spacer temperature against the heat generated rate.

c) Comparison with experimental data.

5.5.5 h VALUE DETERMINATION USING NATURAL CONVECTION THEORY

The values of heat transfer coefficient used to simulate the natural convection conditions in the model was 10 W/m^2K. This h value was verified using an accepted natural convection correlation for a vertical and horizontal surface taking the form;

$$Nu = C(GrPr)^m \tag{5.1}$$

Vertical surface

An accepted value of C and m for a vertical plate in equation 5.1 is C = 0.55 and m = 0.25 [72].

Substituting the relevant values in equation 3.16 (chapter 3) yielded, Grashof number Gr = 22.1, when L is half the height of each level and θ was determined from experiments discussed later. The Pr number for air is approximately constant with the

value of 0.707, for a large variation in pressure and temperature. Therefore equation 5.1 yielded h value of 11.4 W/m^2K.

Horizontal surface

Similarly, for a horizontal surface established correlation, constants are C = 0.54 and m = 0.25, and assuming L to be half of the chip carrier width the h value was calculated to be 6.6 W/m^2K. Therefore the initial estimate of 10 W/m^2K for the vertical surfaces was considered to be reasonable, in that it fell in the range between these two values.

5.5.6 ANALYSIS OF THE SINGLE LEVEL MODEL

The temperature distribution in the model is a function of the surface heat transfer coefficient, convective surface area, material conductivities, model geometry and the power generation. Specifying a constant value of heat transfer coefficient of 10 W/m^2K, and all other model variables remaining constant, the thermal resistance of the model is also constant. This means that the variation in chip temperature, against increasing heat generation rate in the chip should follow a linear pattern.

In a series of FE runs, the power dissipation was varied ranging from 0.125 W to 0.2 W. Figure 5.7 illustrates the temperature distribution of the chip, chip carrier and the plastic spacer for a fixed value of heat transfer coefficient. Similarly Figure 5.8 shows a typical contour plot from the FE corresponding to Figure 5.7. These runs are discussed in detail later. The above FE runs served to validate the self-consistency of the F.E. model itself. The next stage in the validation process, was to compare the FE

predictions to that of the experimental measurements.

5.6 EXPERIMENTAL INVESTIGATION

5.6.1 DESCRIPTION OF THE TEST RIG

Natural convection testing

The test rig to investigate the thermal performance of the chiprack in natural convection is shown in Figure 5.9a. The load resistors on the pulsing board provided a known quantity of power dissipation to each levels chip. As already mentioned, the individual levels temperature was measured using SID described in chapter 4. In addition to SID only for the uppermost level a static infra-red thermometer was used to monitor the temperature of the chip or chip cover.

Forced convection testing

Essentially the only difference between the forced and natural convection test rig, was the placement of the chiprack system in a suitable duct as shown in Figure 5.9b.

5.6.2 OPERATION OF THE CONTROL BOX

Five lines link the pulsing board to the control box. One permanent line carries the SID voltage drop to the pulsing board for sampling. The other four lines can be either connected or disconnected. Each carries signals for one particular level of the chiprack and, if connected, powers that level. Any combination of powered levels may be achieved. However each powered level receives the same input signal and hence the same heat input.

A switch on the control box determines on which level the S.I.D. voltage is being sampled. An isolated input to the control box is the negative measuring voltage, Vm. This is routed to the level where SID voltage measurement is being made.

5.7 EXPERIMENTAL METHOD

5.7.1 VARYING POWER DISSIPATION

The TTL 7400 devices used in the chiprack were real logic devices. This meant that the power dissipation of each level was determined by the value of the load resistors on the pulsing board and pulse train through the logic gates. The gates inverted this signal, so the output signal was measured. An oscilloscope was used to display the pulse train, measured at the output load resistors.

The ratio of the time input is switched to "on", so that the time between pulses is called the Mark Space ratio (MS ratio). The higher the MS ratio, the higher the heat input to the chip. The MS ratio was varied using the pulse width and pulse spacing controls on the pulse generator and set to the required value on the oscilloscope. From the MS ratio of the output signal, it was possible to calculate the heat input to the chip. This calculation is detailed in Appendix A2.

5.7.2 MEASURING TEMPERATURE AT EACH LEVEL

The switch on the control box determined which level is being monitored. The D.V.M. displayed the S.I.D. voltage drop on that level.

The internal construction of the TTL 7400 is shown in Figure 5.10. The TTL 7400 devices one on each level, were calibrated using the procedure described in chapter 4. The SID voltage drop versus temperature is illustrated in Figure 5.11. The SID voltage drop for each level was readily converted to temperature using this chart.

5.8 DETAILS OF EXPERIMENTS CARRIED OUT

The following sets of experiments were carried out on the chiprack using the test rigs.

1) Reduced convection - chiprack insulated.
2) Natural convection - chiprack in ambient conditions.
3) Forced convection - chiprack in duct with horizontal air flow.

5.8.1 REDUCED CONVECTION TEST

Because chiprack is essentially cooled by conduction the reduced convection test was carried out to investigate the effect of conduction in the stack system.

Experimentally the chiprack was insulated by:-

a) Electrical insulating tape and polystyrene foam of thickness 15mm wrapped around the outsides of the stack.

b) Cotton wool on the top of the chiprack.

c) Chiprack motherboard resting on cotton wool and polystyrene foam. Also

cotton wool of thickness 40mm covering the top of the motherboard terminal connections.

Complete insulation of the chiprack cannot, of course be attained. Some conduction of heat through the insulation will still occur. In this condition, all four levels were powered at MS ratios of 10% and 30%. The subsequent temperature of each level was recorded with respect to time (transient analysis).

Tests were also carried out by allowing the stack to convect, while the motherboard was insulated and visa versa.

5.8.2 NATURAL CONVECTION TEST

The chiprack was positioned on the bench top in ambient air. Each level was powered in turn, with MS ratios ranging from 10% to 50%. At each stage, the chiprack was allowed to reach a steady state condition normally within 30 minutes, before the temperature at each level was recorded. Tests were also carried out by removing the chip cover, particularly on the uppermost level to investigate the effect of the chip cover on temperature distribution. Infra-red temperature measurements were also used to assist this test.

To investigate the effect of third level heating, tests were carried out using different combinations of chip carriers at each level in natural convection. To test whether the third level over heating was being caused by hot operating chip carriers, a total of five chip carriers were tested individually as a single level mounted on the mother board. The hottest and coolest chip carriers were identified and used in coolest level (level

1) and the hottest level (level 3).

5.8.3 FORCED CONVECTION TEST

The chiprack was placed in a perspex duct, shown in Figure 5.9b. Tests were performed with air velocities in the duct of 1.0 m/s and 2.0 m/s. Each level of the chiprack in turn was powered with MS (mark space) ratios ranging from 10% to 50%. Experimental data was recorded after steady state conditions were reached. The level of velocities chosen were recommended by Dowty to simulate typical industrial applications of a small fan system.

5.9 PRESENTATION AND DISCUSSION OF RESULTS

5.9.1 RESULTS FROM SINGLE LEVEL FE MODEL

The isothermal contour plots showing the effect of varying the heat transfer coefficient are illustrated in Figures 5.11 to 5.16. Analysis of these figures show that the contour lines are closely packed together at the chip indicating a high heat flux region, the magnitude of the flux is reduced towards the edge of the carrier. Since the only heat sink in this model is the convection on the sides of the stack, the heat is conducted along the carrier towards the plastic spacer.

The FE runs with high values of heat transfer coefficient, 25 W/m^2K and above, show a distortion of the contour lines towards the chip, about a quarter of the way from the centre, along the line of symmetry of the model. This was not a "real" effect. It was due to the ANSYS package exhibiting inaccuracy when dealing with elements that

have a very long length to thickness ratio. Investigation of this effect by removing some "thin" elements showed that the effect was localised and did not affect the chip temperature significantly. This fault was rectified in the one eighth model.

The heat transfer under the chip cover can be complicated. The air layer between the chip heat source and the chip cover, constitutes a thin layer of fluid between two plates heated from below. This is a classical case of unstable natural convection. If the Rayleigh number Ra is low, the fluid conducts as a solid and no convection current develops. Buoyancy forces are resisted by viscous forces and dissipated by conduction. At a critical value of Ra, the buoyancy forces overcome these effects, and convection cells will develop. Accurate analysis of this part of the model will therefore require a fluid model to study the already mentioned effects and lies beyond the scope of the present work.

5.9.2 RESULTS FROM FOUR LEVEL FE MODEL

The isothermal contour plots of four level FE model, powering each level at a time are shown in Figures 5.17 and 5.18. The analyses of these figures show that, heat travels horizontally along the chip carrier of the powered level, similar to single level FE model.

Level one powered only

When level one is powered, the motherboard was shown to act as a heat sink. Despite the convection applied to the top surface of the uppermost level and sides of the stack, the heat transfer to the upper levels was not shown to be significant, suggesting that

the lowest level was being cooled mainly by conduction.

Level two powered only

Analysis of the temperature distribution, when this level powered, was similar to level three powered on its own. In both cases, the temperature of the level below the powered level was higher than the level above it. This further suggested that the stack may mainly be cooling by conduction and was investigated experimentally and discussed later.

Level four powered only

Analysis of this level shows that level four was being cooled mainly by convection. The effect of this level powered on unpowered levels is summarised in table 5.3.

The temperatures, both from the FE runs and experiments for varying power dissipation, are shown in Tables 5.2 and 5.3.

All levels powered simultaneously

When all levels were powered, the heat loss from the motherboard was shown to be more significant compared to that from the top and the sides of the stack, with almost all of the heat travelling downwards towards the motherboard. The analysis showed that the third level operated at the higher temperature compared to other levels. This would be expected if the stack was being cooled by conduction, mainly because it was the furthest level from the motherboard. Furthermore, it was found that the first level operated the coolest, because it was the nearest level to the motherboard. Comparison of the FE prediction and experimental measurements are shown in Figure 5.19 and Table 5.4.

Analysis of Figure 5.19 shows that the heat transfer coefficient even at 10 W/m^2K is too high, because the FE predictions are much lower than the experimental measurements for the fourth level. Furthermore the experimental data also indicate that the third level is the hottest level.

This was further investigated both experimentally and by transient FE analysis.

5.9.3 RESULTS FROM TRANSIENT ANALYSIS

Figure 5.20a and 5.20b illustrate the temperature of each level against time, with the chiprack heavily insulated. The FE model of the four levels was also modified to perform transient analysis. Corresponding FE predictions are shown in Figures 5.21. Comparison of the FE predictions and the experimental measurements show that better agreement was achieved when the convection was reduced. Furthermore, both the FE and experimental data indicate that level three did run the hottest, as noted in earlier analysis. This would suggest that the stack apart from level four was mainly being cooled by conduction.

Figure 5.22 illustrates the transient temperature response, when all levels were powered and the motherboard heavily insulated, whilst the sides and the top surface of the uppermost level was allowed natural convection. In Figure 5.22 comparison of the temperature profiles shows that, levels one, two and three are marginally effected, whilst level four did experience some cooling. Similarly Figure 5.23 depicts transient temperature response, when all levels were powered with sides and the top surface of the uppermost level heavily insulated. It was noted that in the latter case the

temperature of the chip at level four was approximately 10% higher than that at level three.

Figure 5.24 illustrates the transient response of the chip temperature when all levels powered were in natural convection. Similarly Figure 5.25 shows the normalized responses of the four levels corresponding to Figure 5.24. Analysis of this Figure proclaim that the rate of heat generation at each level is that same. Furthermore 50% of the steady state temperature of each level is reached in the first five minutes, and almost 85% in the next five minutes.

5.9.4 RESULTS FROM NATURAL CONVECTION ANALYSIS

The steady state temperatures were obtained at each level in natural convection. The general trend with increasing power dissipation (MS ratio 0 to 50%) was still the same (third level running at a higher temperature compared to other levels).

Tables 5.5 and 5.6 illustrate the steady state temperature reached at each level when rotation of the chip carriers was carried out. Despite any combination of the chip carriers, level 3 operated the hottest and level 1 the coolest. This further suggested that level four was the only level mainly being cooled by convection.

Figure 5.26 shows the temperature of each level with chip cover in place and removed. As illustrated, the chip cover removal had a marginal effect on the chip temperature and did not promote convection.

Comparison of IR and SID for level four is also shown in Figure 5.27.

5.9.5 RESULTS FROM FORCED CONVECTION

Figures 5.28 a-d illustrate the steady state temperature of the chip in forced convection when each level was powered in turn. Analysis of these figures showed that at high power dissipation (50% MS ratio) and maximum velocity used (2 m/s), level 1 and level 2 achieved a temperature reduction of 5°C. Level three achieved a 7°C temperature reduction and level four a 10°C temperature reduction compared to the temperature of the stack in natural convection in the duct.

The results from forced convection tests once again showed that the chiprack stack was being cooled by conduction and convection on the uppermost level, and mainly by conduction on all subsequent levels.

5.10 CONCLUSION

The objectives to investigate the thermal performance of the chiprack were achieved. The FE model was validated, and in general produced good agreement with the experimental measurements. Outputs from FE, revealed the complex temperature distribution within the chiprack stack system. The SID described in (chapter 4) was used and proved to be the only possible method of temperature measurement that could be applied to the investigation of a chiprack system with an unencapsulated chip carrier.

The thermal performance of the chiprack four level system was investigated experimentally. In general it can be concluded that the stack system was being cooled largely by conduction, apart from the upper most level which was found to be cooling both by conduction and convection.

Experiment showed that the temperature levels were not affected by changing individual carriers. It was also demonstrated that the chip covers have no significant effect on promoting convection if removed.

First level powered

POWER (W)	0.13	0.14	0.16	0.17	0.19	0.50
LEVEL 1 TEMP: • C						
FE	17.01	19.9	22.5	26.8	28.9	32.31
EXP *	18.0	21.0	24.5	28.0	31.0	-
LEVEL 2 TEMP: • C						
FE	3.29	3.70	4.10	4.50	4.89	13.16
EXP	2.00	3.00	3.21	3.50	4.0	-
LEVEL 3 TEMP: • C						
FE	1.79	2.02	2.24	2.45	2.67	6.96
EXP	0.50	0.62	0.69	0.72	0.75	-
LEVEL 4 TEMP: • C						
FE	0.29	0.33	0.36	0.39	0.43	1.29
EXP	0.0	0.0	0.12	0.13	0.38	-

* Exp = Experimental results

Second level powered

POWER (W)	0.13	0.14	0.16	0.17	0.19	0.50
LEVEL 1 TEMP: • C						13.2
FE	2.29	3.5	4.00	4.50	4.90	-
EXP *	1.12	2.0	2.85	3.10	3.83	
LEVEL 2 TEMP: • C						31.5
FE	16.0	19.2	21.0	25.68	27.8	-
EXP	18.0	21	25.0	27.0	29.5	
LEVEL 3 TEMP: • C						10.3
FE	2.75	2.89	3.75	4.12	4.45	-
EXP	1.75	3.0	2.50	2.68	2.75	
LEVEL 4 TEMP: • C						2.41
FE	0.60	0.68	0.75	0.83	0.90	-
EXP	1.00	1.00	1.50	1.12	1.00	

* Exp = Experimental results

TABLE 5.2 - EXPERIMENTAL AND FE PREDICTION OF CHIP TEMPERATURE FROM FE FOUR LEVEL MODEL, WHEN INDIVIDUAL LEVELS POWERED IN TURN (DEG. C) ABOVE AMBIENT, NATURAL CONVECTION TEST.

Third level powered

POWER (W)	0.13	0.14	0.16	0.17	0.19	0.50
LEVEL 1 TEMP: • C						7.3
FE	1.21	1.25	1.98	2.10	2.56	-
EXP *	0.0	0.0	0.0	0.0	0.0	
LEVEL 2 TEMP: • C						10.3
FE	2.60	2.90	3.20	3.35	3.80	-
EXP	3.00	2.89	2.89	2.89	3.00	
LEVEL 3 TEMP: • C						26.7
FE	15.5	17.4	20.1	23.54	26.6	-
EXP	17.9	21.0	23.5	26.5	29.5	
LEVEL 4 TEMP • C						3.65
FE	0.90	1.1	1.14	1.25	1.36	-
EXP	1.00	1.0	1.00	1.00	1.65	

* Exp = Experimental results

Fourth level powered

POWER (W)	0.13	0.14	0.16	0.17	0.19	0.50
LEVEL 1 TEMP: • C						
FE	0.30	0.32	0.36	0.39	0.43	1.15
EXP *	0.00	0.0	0.00	0.00	0.00	-
LEVEL 2 TEMP: • C						
FE	0.60	0.67	0.80	0.83	0.89	2.40
EXP	0.00	0.12	0.50	0.55	0.56	-
LEVEL 3 TEMP: • C						
FE	0.90	1.03	1.14	1.30	1.36	3.65
EXP	1.00	1.00	1.0	1.00	1.10	-
LEVEL 4 TEMP: • C						
FE	12.89	14.2	17.3	19.8	21.8	18.2
EXP	15.5	18.0	21.0	23.5	26.0	-

* Exp = Experimental results

TABLE 5.3- EXPERIMENTAL AND FE PREDICTION OF CHIP TEMPERATURE FROM FE FOUR LEVEL MODEL, WHEN INDIVIDUAL LEVELS POWERED IN TURN (DEG. C) ABOVE AMBIENT, NATURAL CONVECTION TEST.

All levels powered

POWER (W)	0.13	0.14	0.16	0.17	0.19	0.50
LEVEL 1 TEMP: ° C FE EXP *	15.7 15.0	17.7 20.0	19.6 24.5	21.5 27.5	23.4 30.0	34.4 -
LEVEL 2 TEMP: ° C FE EXP	16.6 14.5	18.7 20.0	20.7 25.0	22.7 29.0	24.7 32.0	56.8 -
LEVEL 3 TEMP: ° C FE EXP	14.2 17.0	16.0 23.0	17.7 29.0	19.4 34.0	21.1 37.5	66.3 -
LEVEL 4 TEMP: ° C FE EXP	8.60 16.0	9.7 22.0	10.4 27.0	11.8 32.0	12.8 35.5	62.8 -

* Exp = Experimental results

TABLE 5.4 - EXPERIMENTAL AND FE PREDICTION OF CHIP TEMPERATURE FROM FE FOUR LEVEL MODEL, ALL LEVELS POWERED (DEG. C) ABOVE AMBIENT, NATURAL CONVECTION TEST.

MS RATIO	LEVEL NUMBER	CHIP CARRIER NUMBER	CHIP TEMPERATURE °C
0%	4	5	41
	3	1	43
	2	2	42
	1	4	42
10%	4	5	49
	3	1	51
	2	2	50
	1	4	48
20%	4	5	55
	3	1	58
	2	2	57
	1	4	54
30%	4	5	63
	3	1	66
	2	2	64
	1	4	58
40%	4	5	70
	3	1	75
	2	2	71
	1	4	65
50%	4	5	77
	3	1	83
	2	2	79
	1	4	70

Table 5.5a - ROTATION OF CHIP CARRIERS AT EACH LEVEL

MS RATIO	LEVEL NUMBER	CHIP CARRIER NUMBER	CHIP TEMPERATURE °C
0%	4	2	45
	3	4	47
	2	5	46
	1	1	42
10%	4	2	47
	3	4	52
	2	5	50
	1	1	44
20%	4	2	55
	3	4	60
	2	5	59
	1	1	50
30%	4	2	61
	3	4	68
	2	5	66
	1	1	55
40%	4	2	68
	3	4	75
	2	5	72
	1	1	60
50%	4	2	74
	3	4	84
	2	5	80
	1	1	64

Table 5.5b- ROTATION OF CHIP CARRIERS AT EACH LEVEL

FIGURE - 5.1 CHIPRACK STACK ASSEMBLY

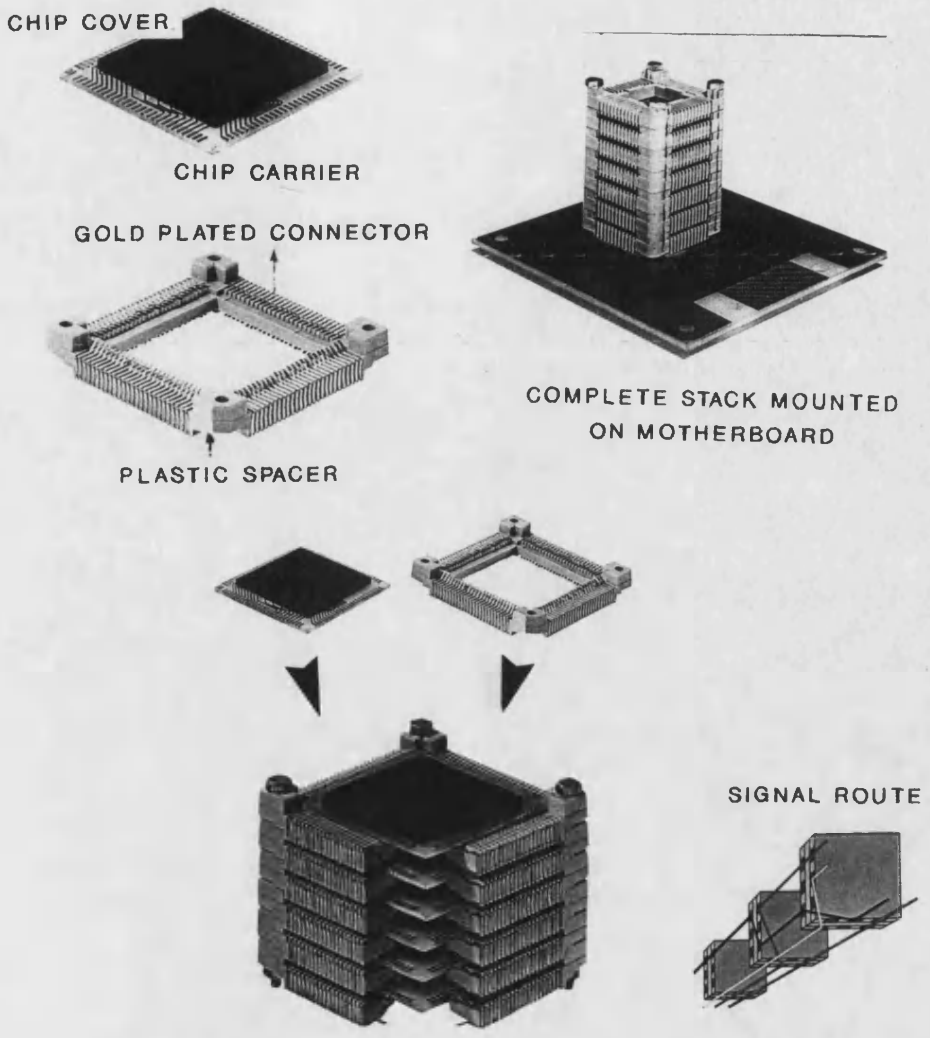
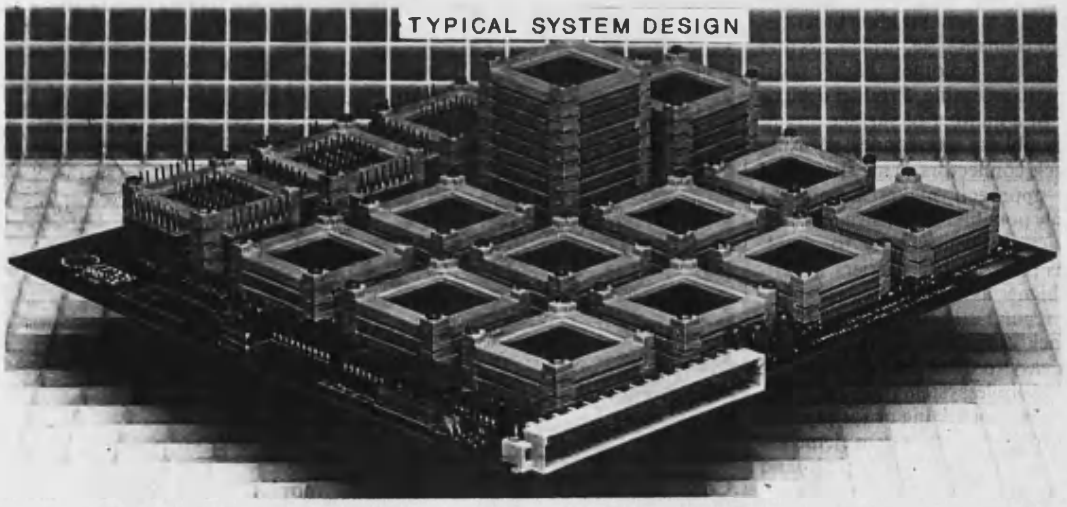


FIGURE - 5.2 TYPICAL SYSTEM CONNECTION ASSEMBLY



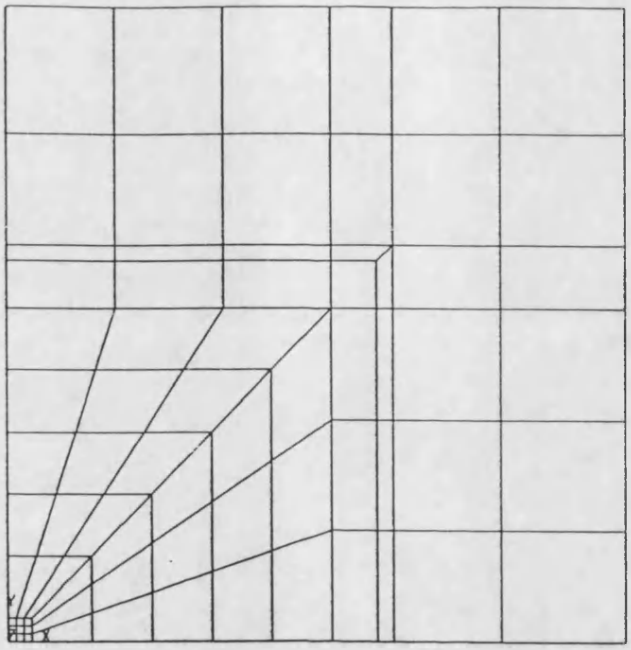


FIGURE 5.3
1/4 SINGLE LEVEL
MESH PLAN VIEW

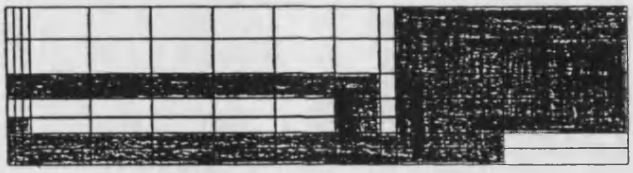


FIGURE 5.4, 5.5
- MESH SIDE VIEW
(1/4 AND 1/8 MODEL)

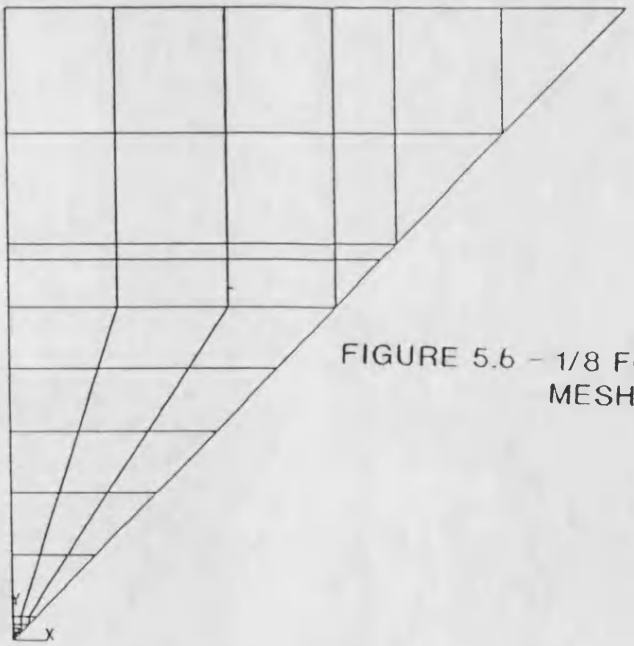


FIGURE 5.6 - 1/8 FOUR LEVEL MODEL
MESH PLAN VIEW

FIGURE 5.7

INTERNAL HEAT GENERATION vs TEMPERATURE RISE OF DIFFERENT PARTS OF THE FE MODEL h COEFFICIENT 10 W/m^2K SINGLE LEVEL

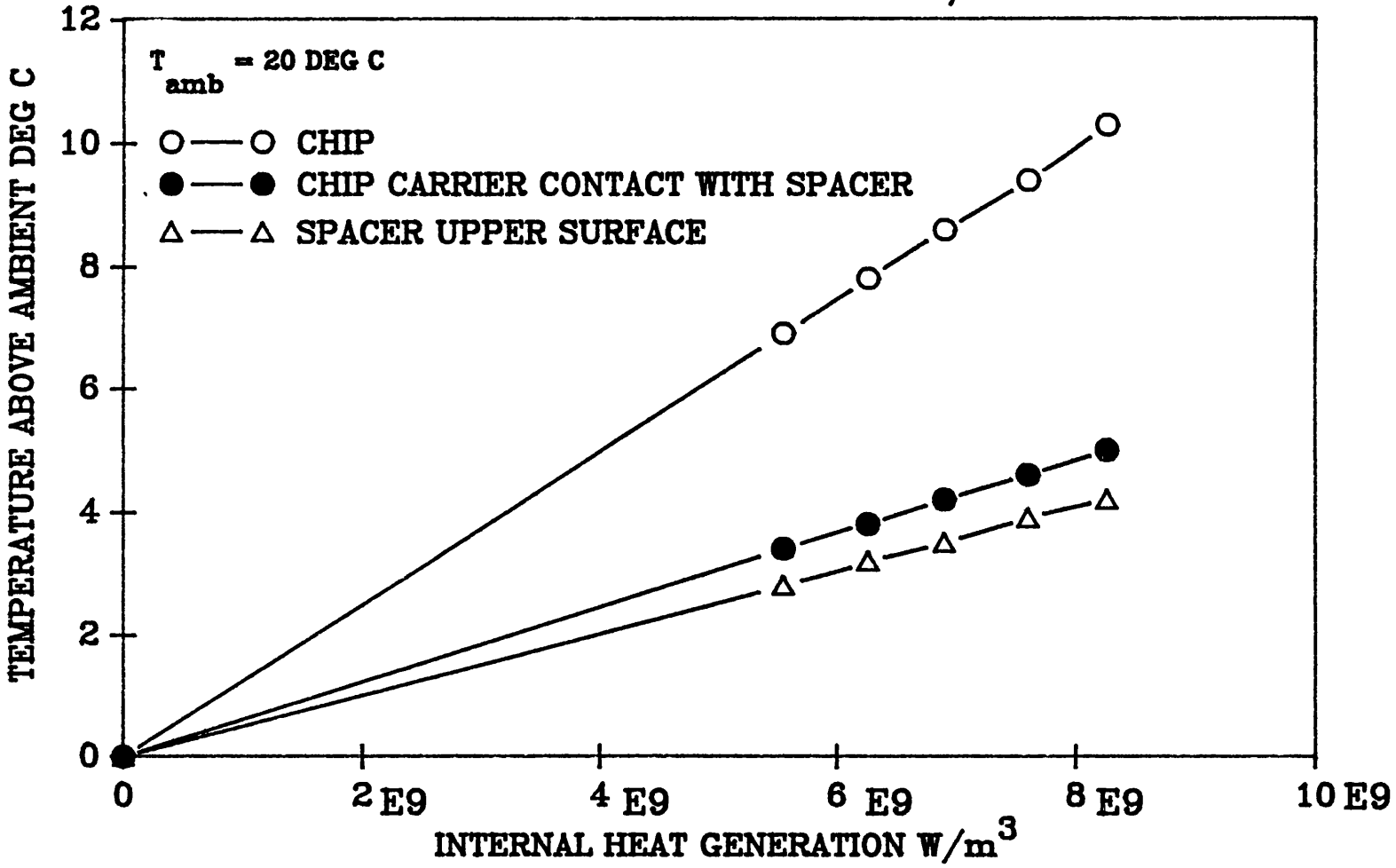
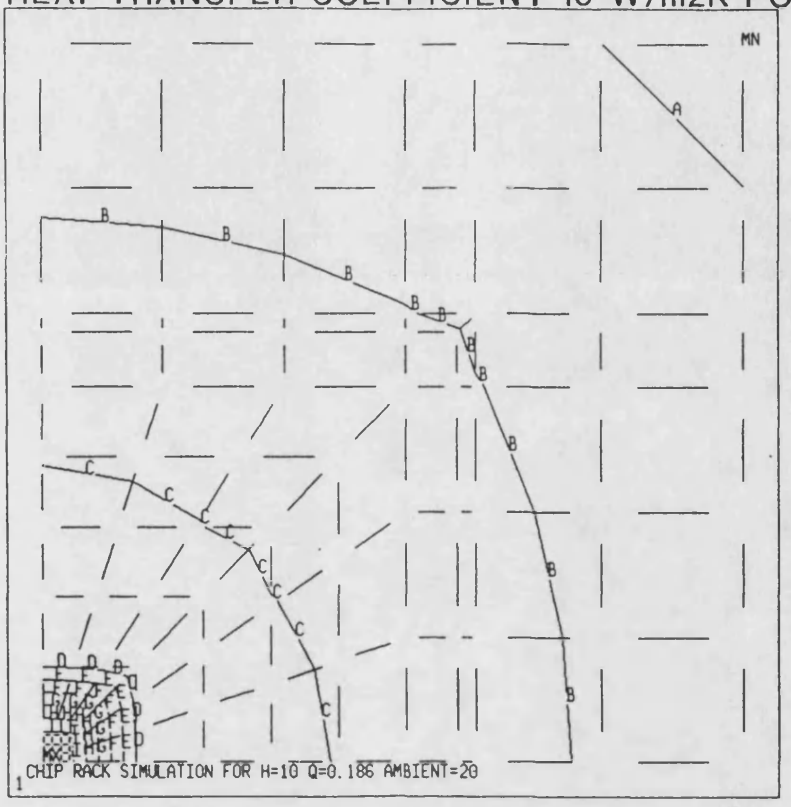


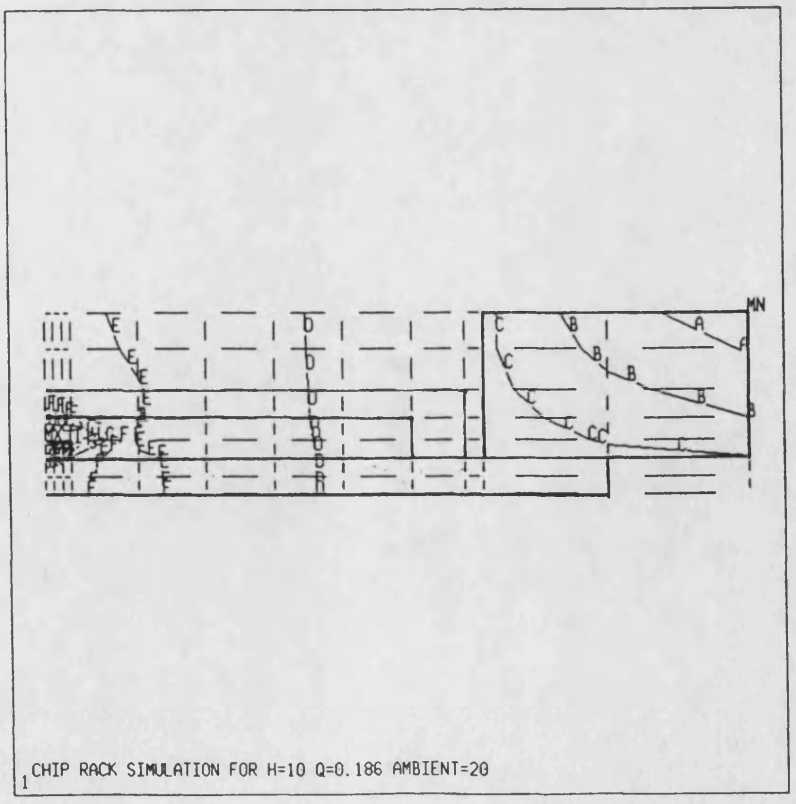
FIGURE 5.8
- TEMPERATURE CONTOUR PLOT SINGLE LEVEL MODEL
HEAT TRANSFER COEFFICIENT 10 W/m2K POWER 0.19 W



POST1 STRESS
STEP=1
ITER=1
TEMP

ZV=1
DIST=.011
XF=.01
YF=.01
ZF=.0035
SECTION
MX=30.3
MN=24.2
A=24.4
B=25.1
C=25.8
D=26.5
E=27.2
F=27.9
G=28.6
G=28.6
I=30

Vertical section through the chiprack



POST1 STRESS
STEP=1
ITER=1
TEMP

YV=1
DIST=.011
XF=.01
ZF=.00251
SECTION
MX=30.3
MN=23.1
A=23.5
B=24.3
C=25.1
D=25.9
E=26.7
F=27.5
G=28.3
H=29.1
I=29.9

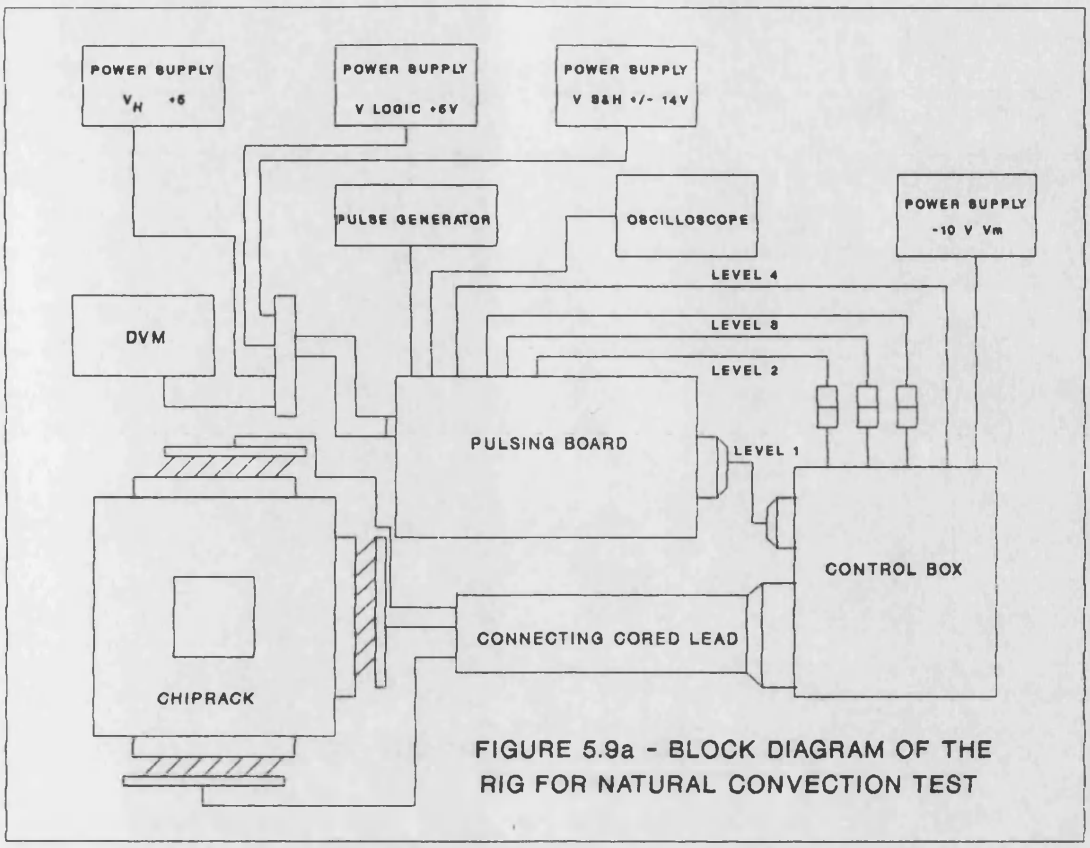


FIGURE 5.9a - BLOCK DIAGRAM OF THE RIG FOR NATURAL CONVECTION TEST

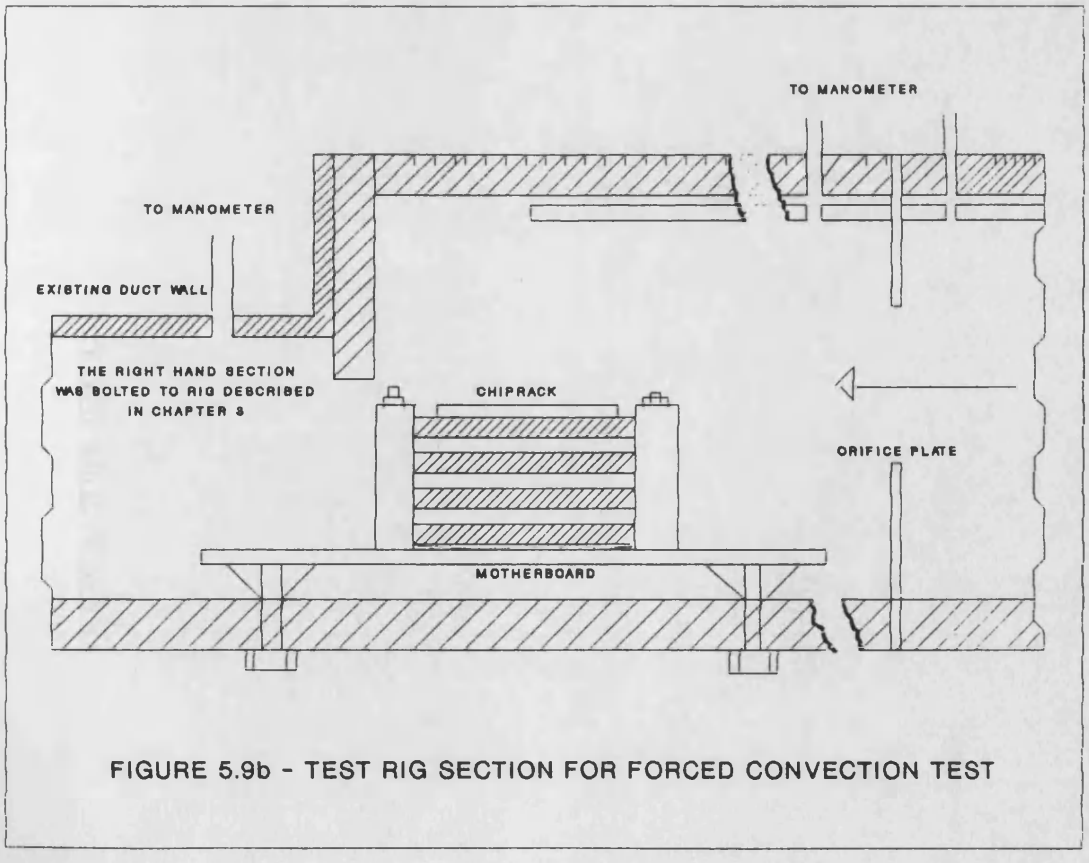


FIGURE 5.9b - TEST RIG SECTION FOR FORCED CONVECTION TEST

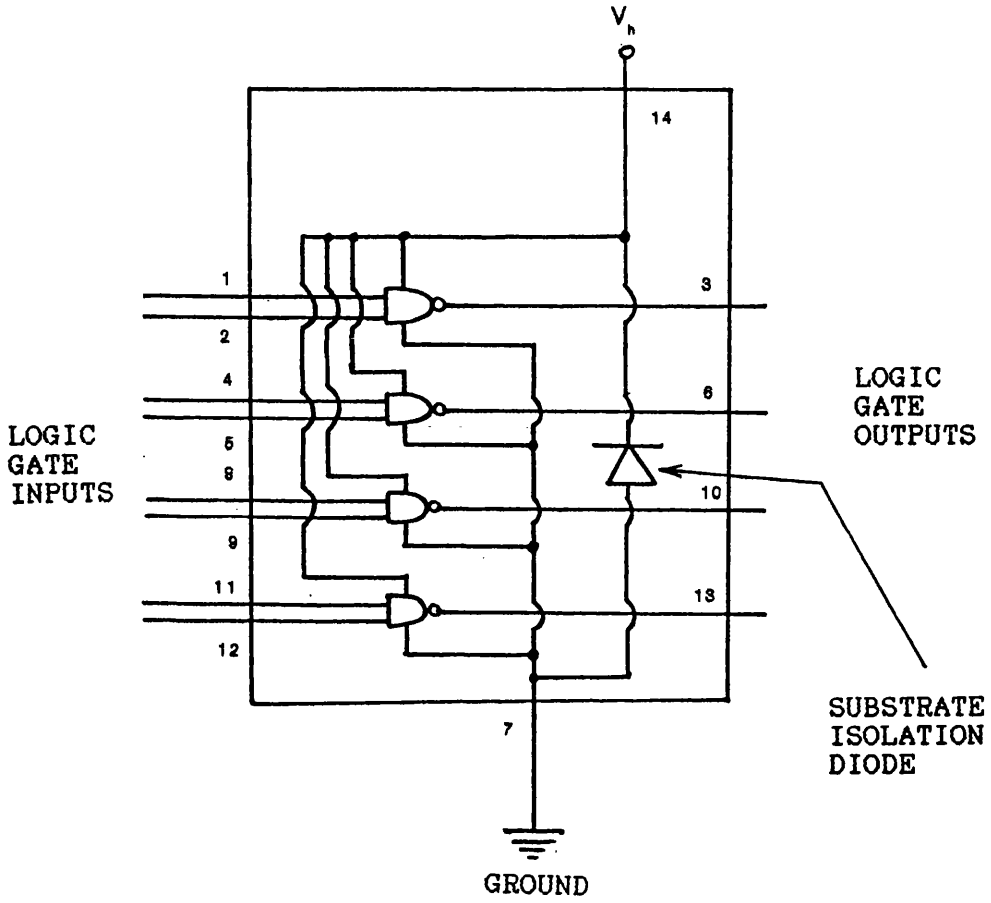


FIGURE 5.10 - A TYPICAL LOGIC DEVICE (TTL7400)
INTERNAL CONSTRUCTION

FIGURE 5.11

CALIBRATION OF TTL 7400 TEMPERATURE vs SID READING

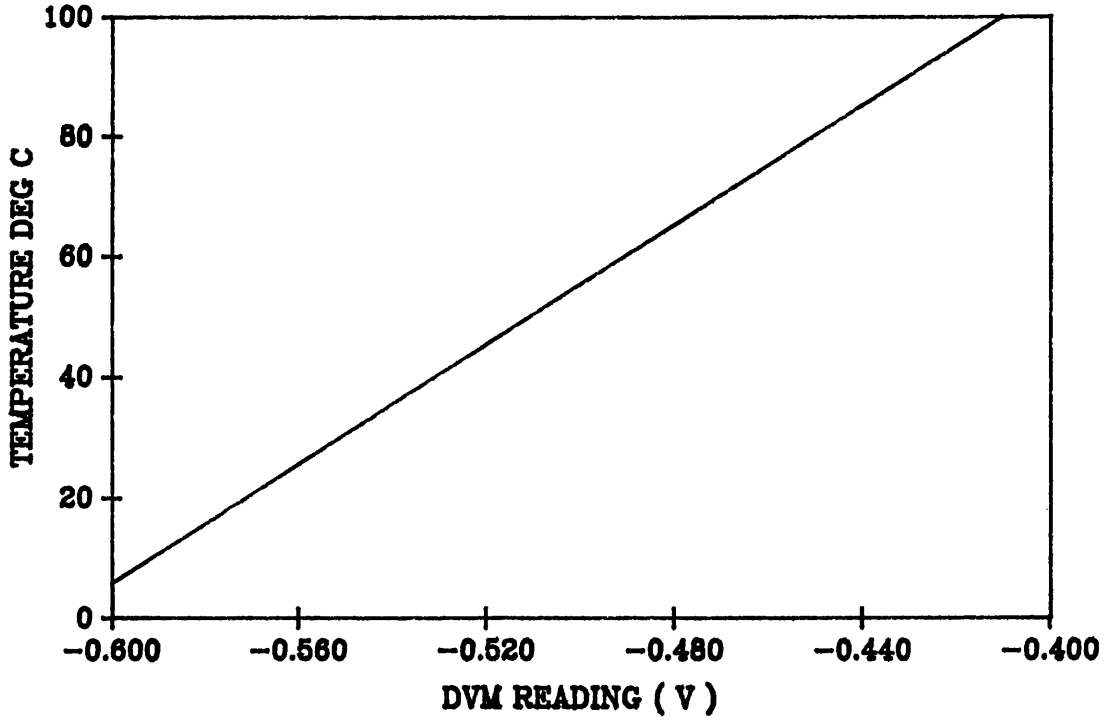
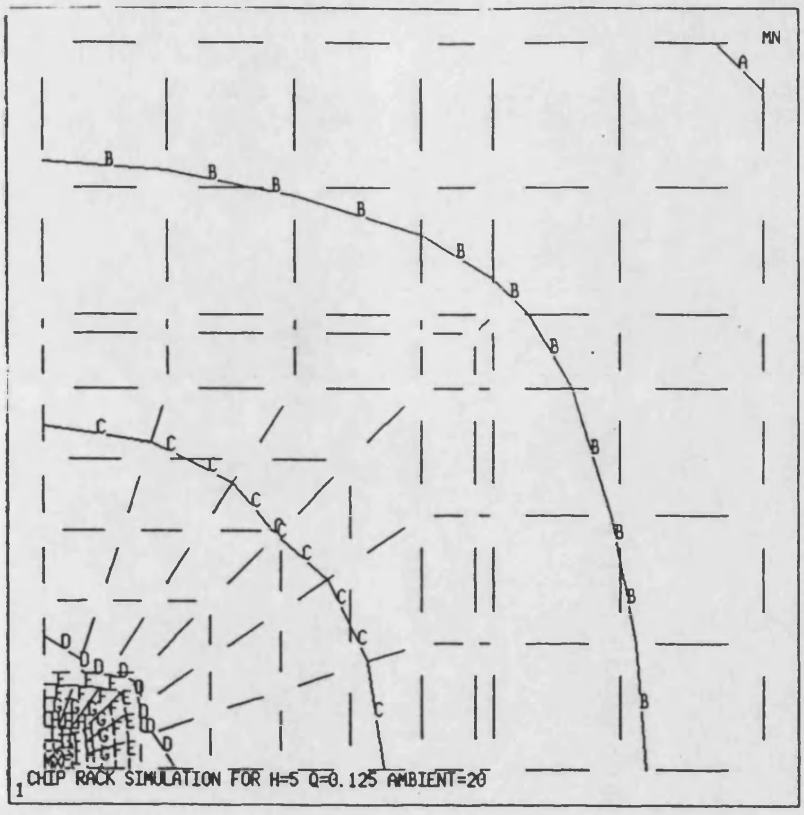


FIGURE 5.12 - TEMPERATURE DISTRIBUTION ALONG THE CHIP CARRIER, SINGLE LEVEL MODEL P=0.13W h=5 W/M^2 K



Vertical section through the chiprack

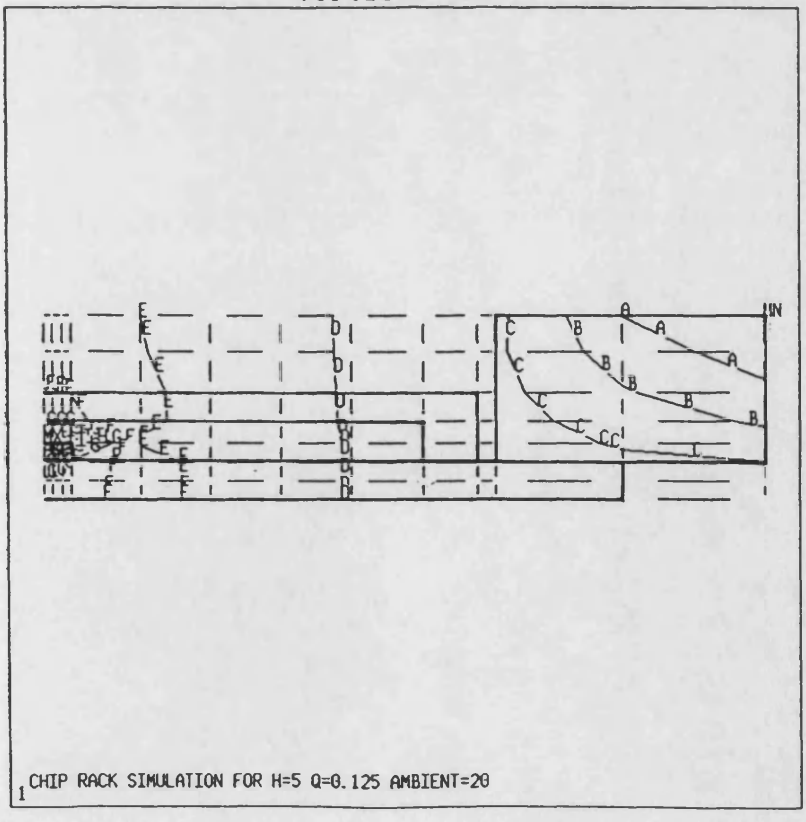
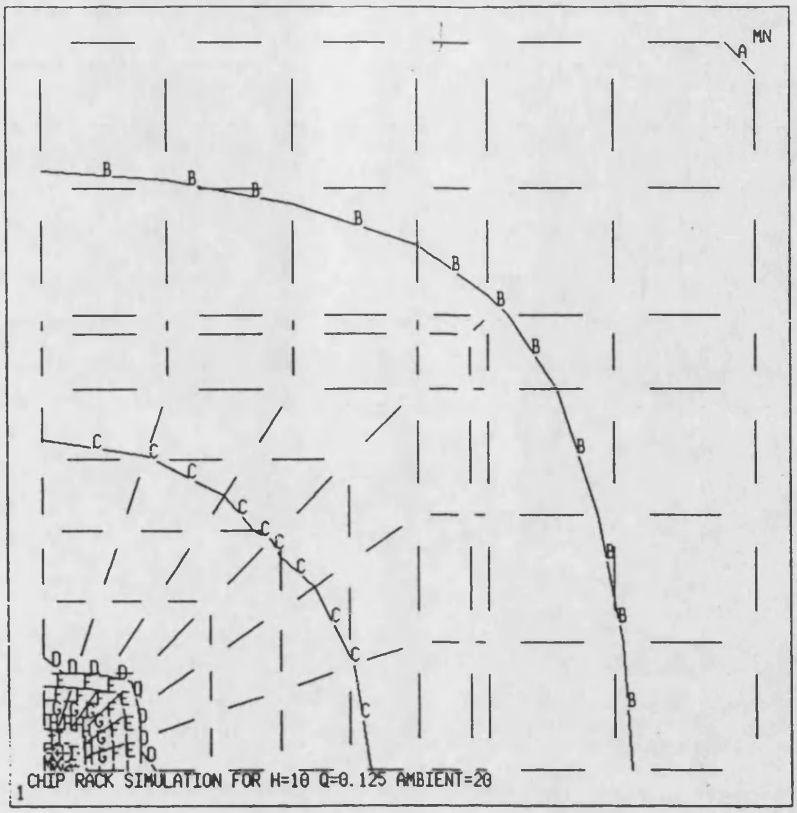


FIGURE 5.13 - TEMPERATURE DISTRIBUTION ALONG CHIP CARRIER, SINGLE LEVEL MODEL P=0.13 h=10 W/m^2 K



Vertical section through the chiprack

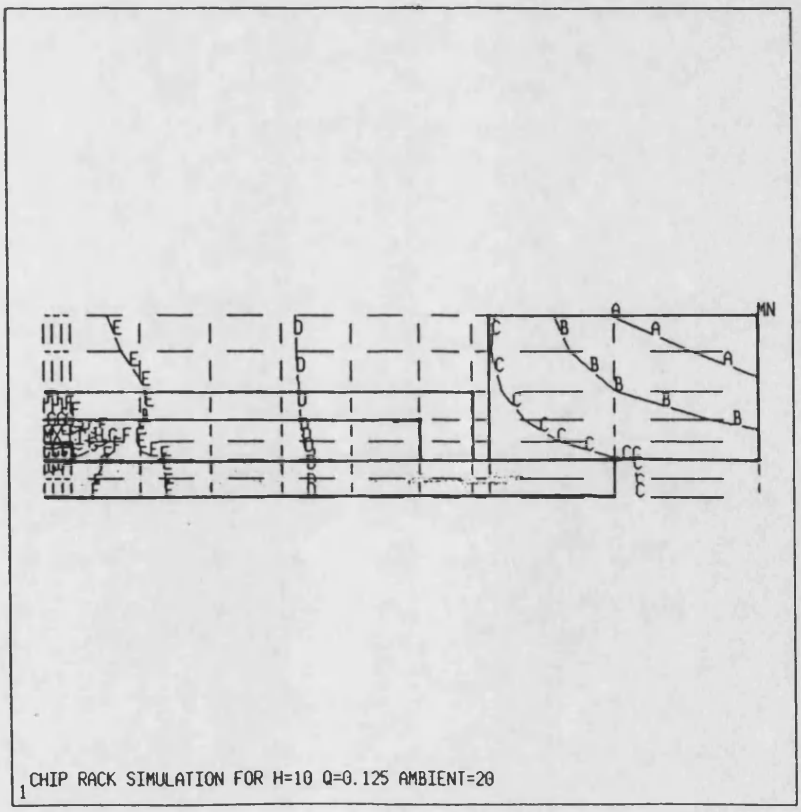
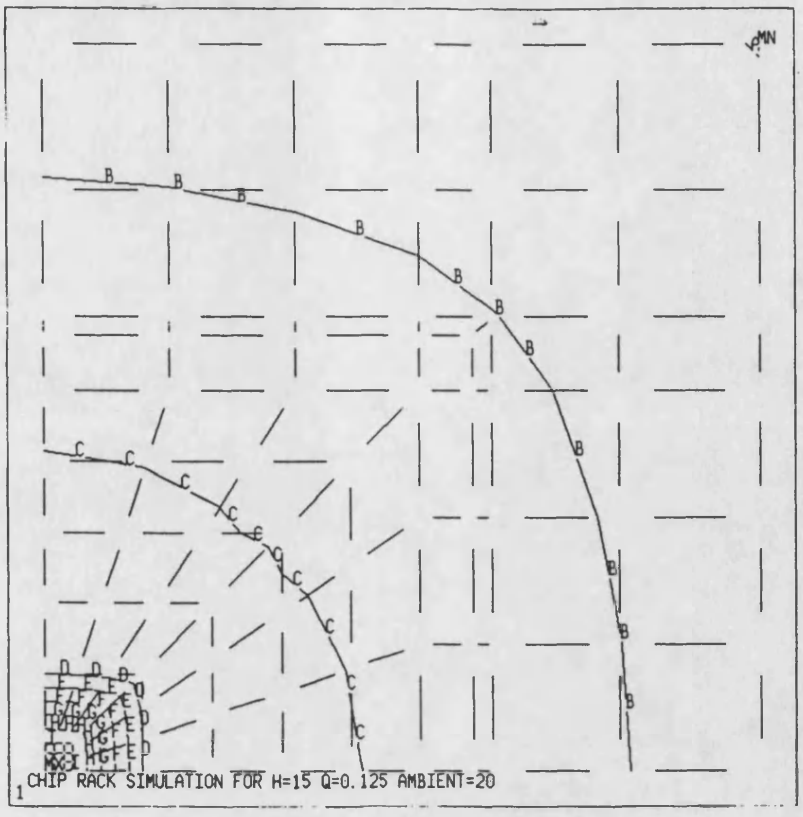


FIGURE 5.14 - TEMPERATURE DISTRIBUTION ALONG CHIP CARRIER, SINGLE LEVEL MODEL P=0.13 h=15 W/m^2 K



Vertical section through the chiprack

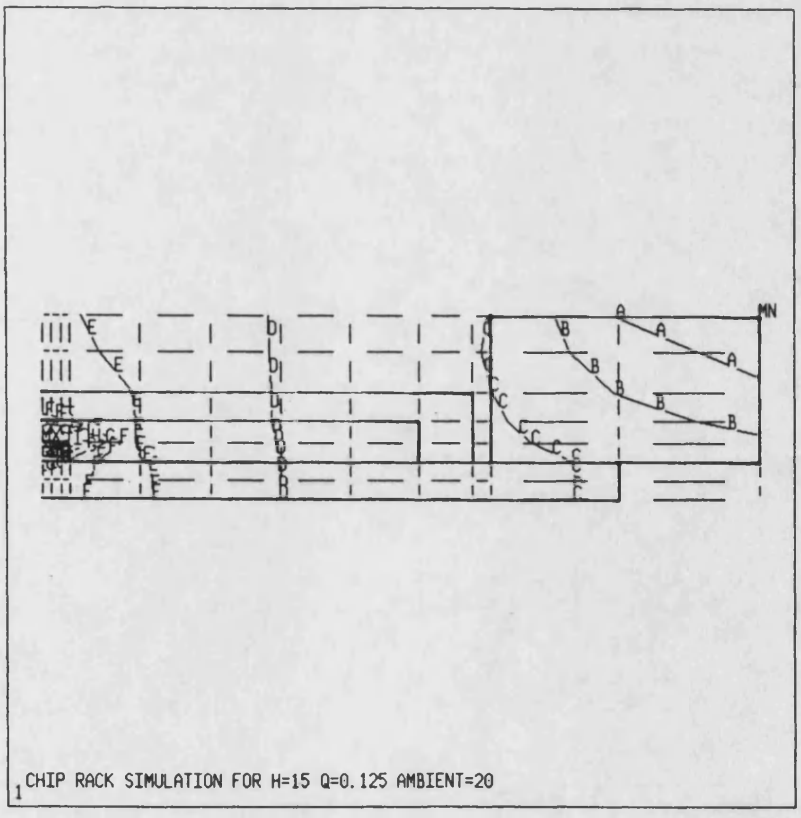
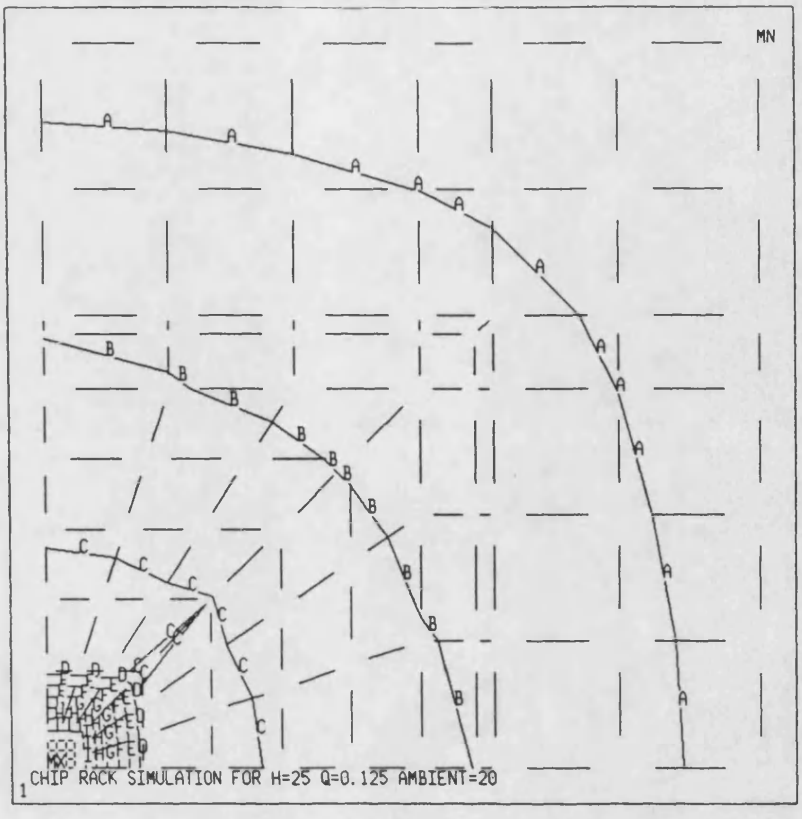


FIGURE 5.15 - TEMPERATURE DISTRIBUTION ALONG CHIP CARRIER, SINGLE LEVEL MODEL P=0.13 h=25 W/m^2 K



Vertical section through the chiprack

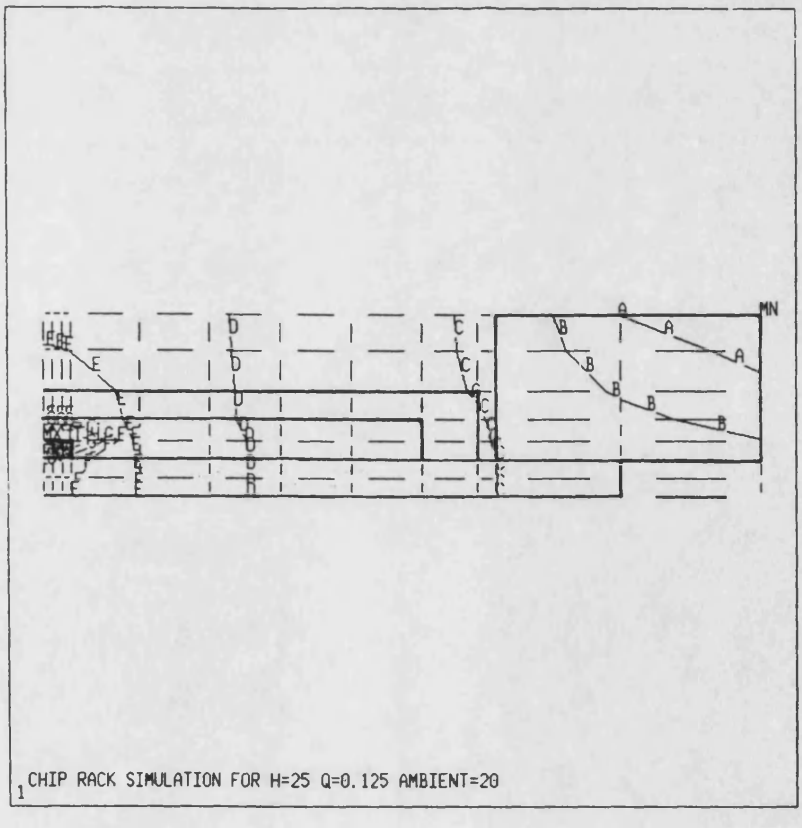
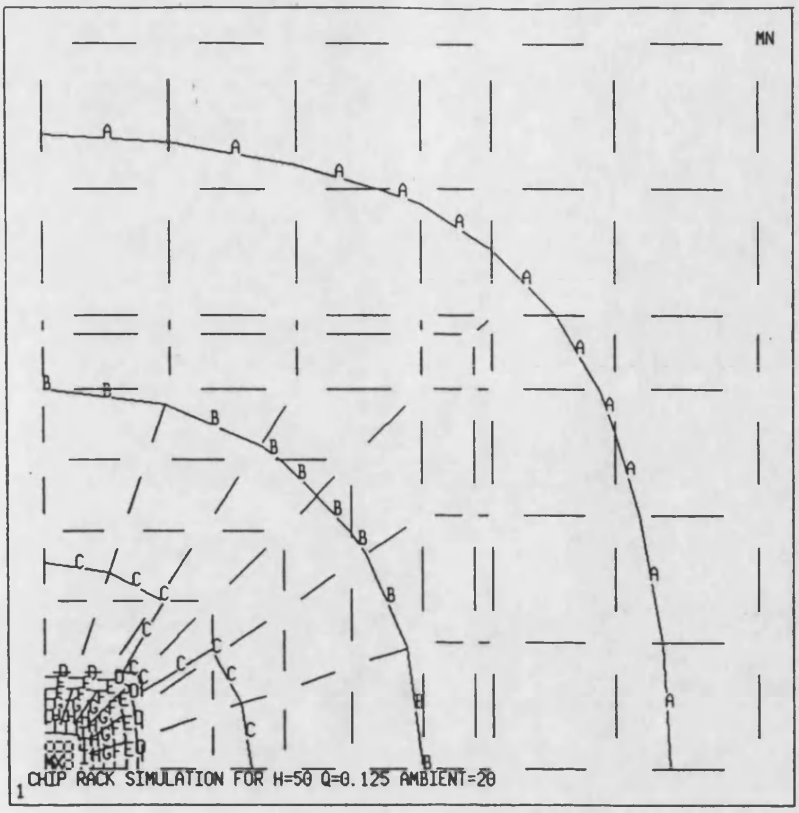


FIGURE 5.16 - TEMPERATURE DISTRIBUTION ALONG CHIP CARRIER, SINGLE LEVEL MODEL P=0.13 h=50 W/m^2 K



Vertical section through the chiprack

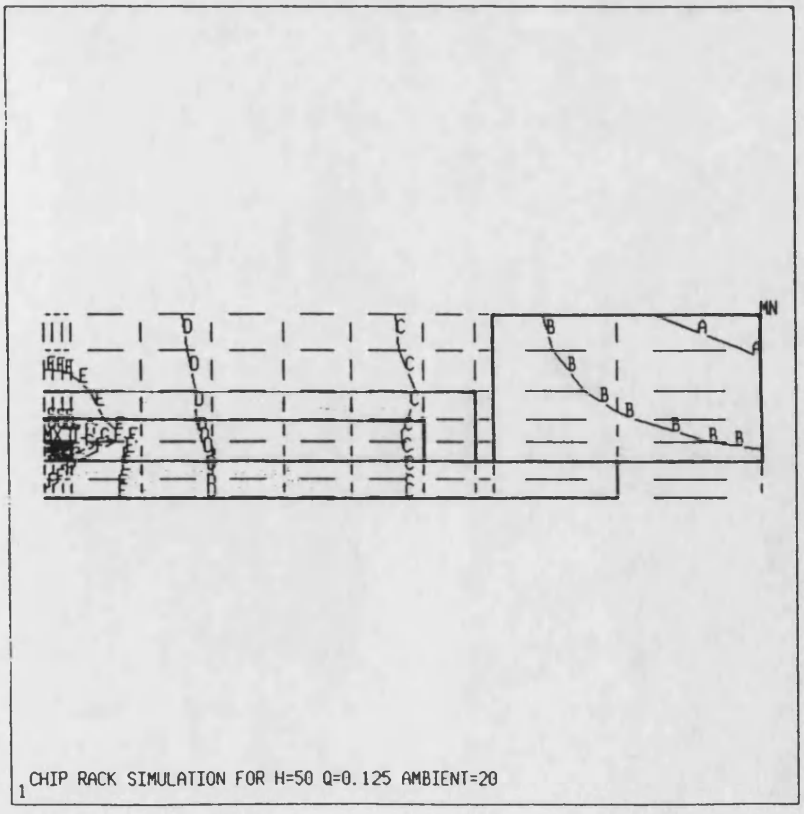
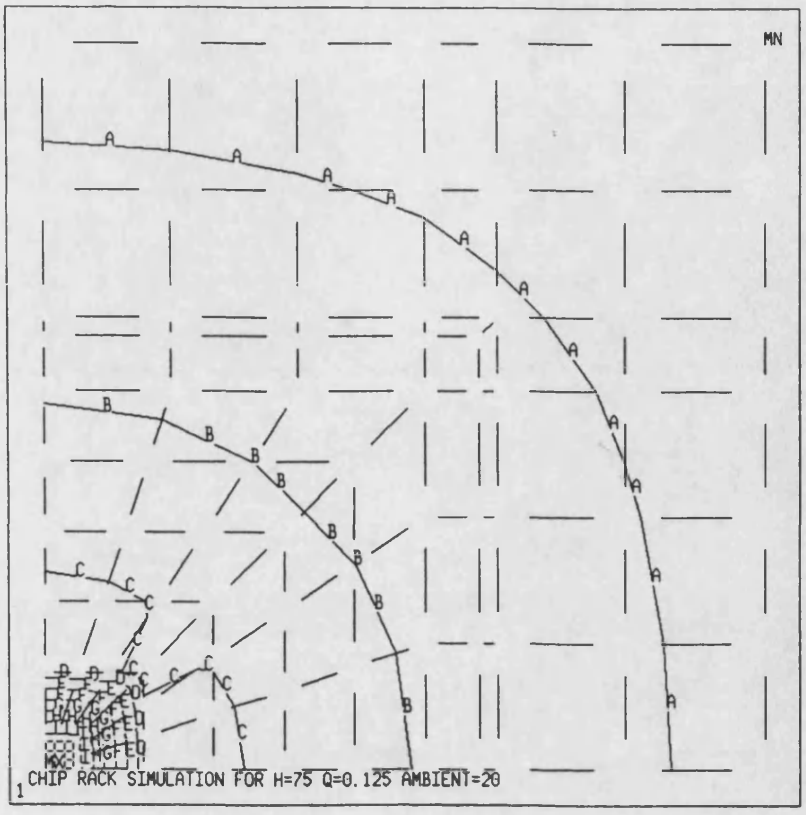


FIGURE 5.17 - TEMPERATURE DISTRIBUTION ALONG CHIP CARRIER, SINGLE LEVEL MODEL P=0.13 h=75 W/m^2 K



Vertical section through the chiprack

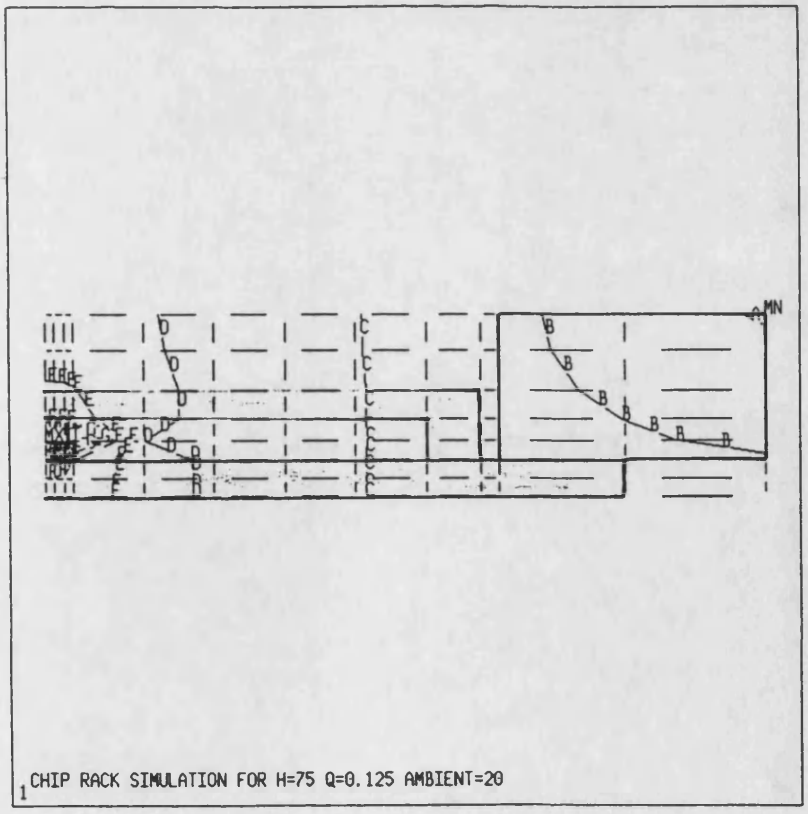
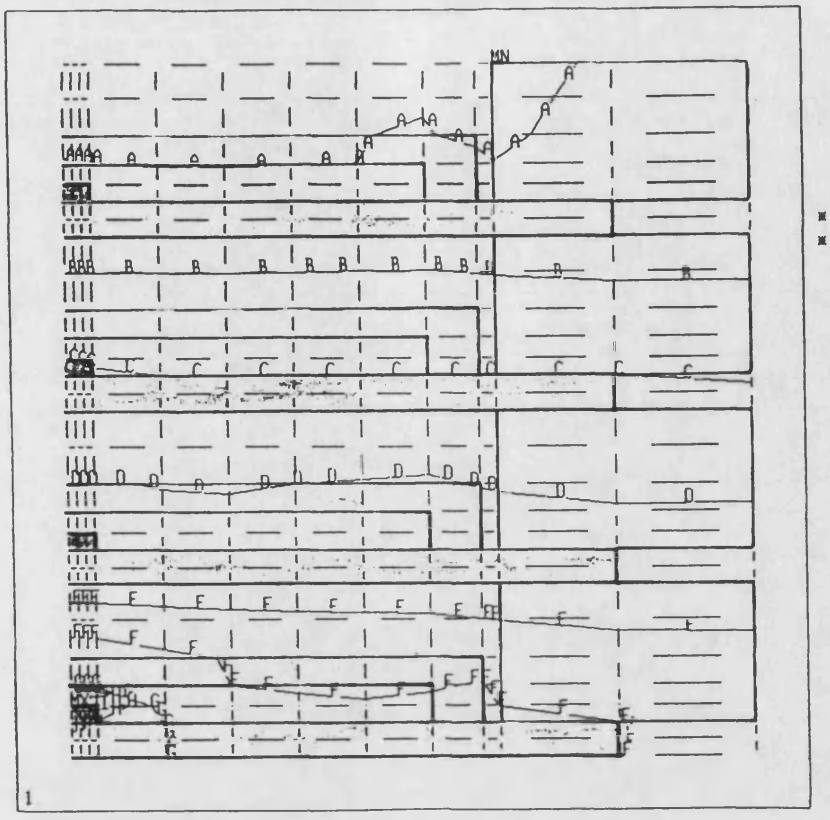


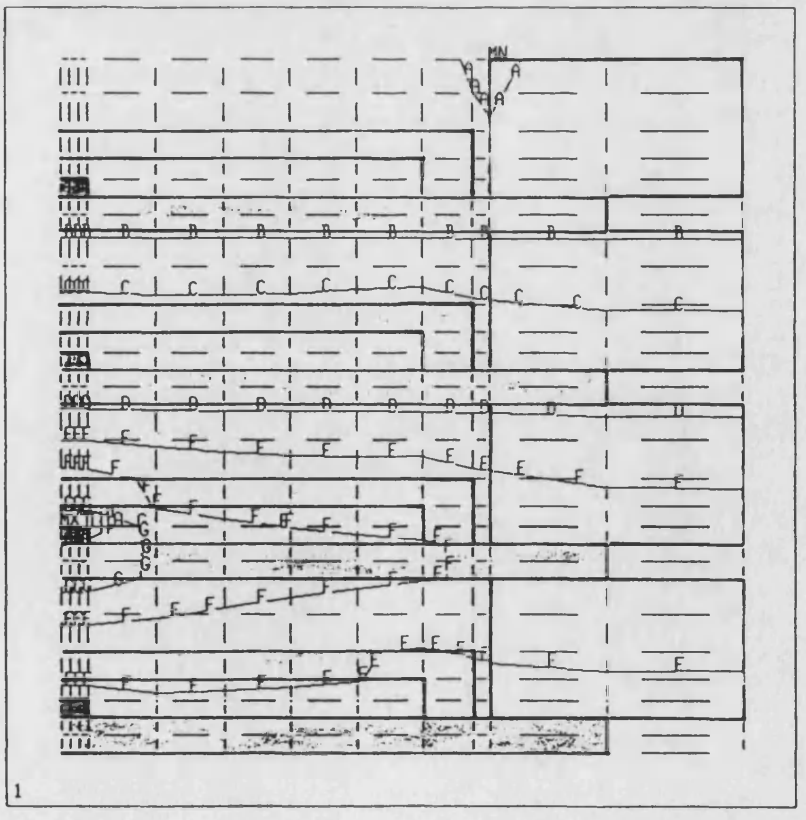
FIGURE 5.18a - VERTICAL SECTION CONTOUR PLOT FOUR LEVEL MODEL. LEVEL 1 POWERED 0.5W, h = 10Wm^2 K



POST1 STRESS
TEMP

YV=1
DIST=.0116
XF=.01
ZF=.0101
SECTION
MX=52.3
MN=18
A=19.2
B=23.2
C=27.2
D=31.2
E=35.2
F=39.2
F=39.2
G=43.2
I=51.2

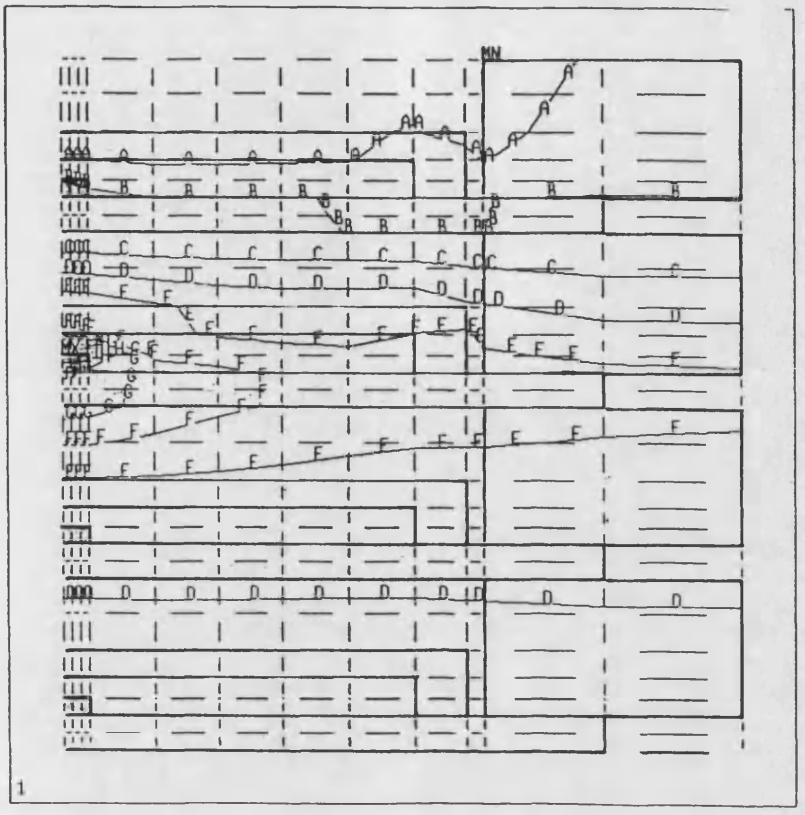
FIGURE 5.18b - SIMILAR TO 18a LEVEL 2 POWERED



POST1 STRESS
TEMP

YV=1
DIST=.0116
XF=.01
ZF=.0101
SECTION
MX=51.5
MN=18.3
A=18.9
B=22.9
C=26.9
D=30.9
E=34.9
E=34.9
F=38.9
G=42.9
I=50.9

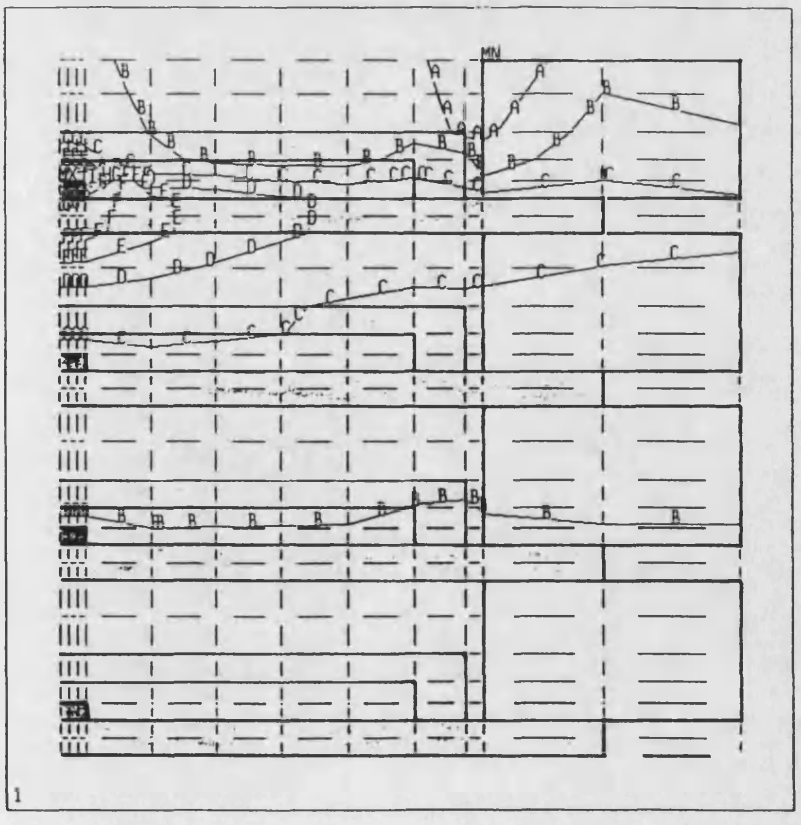
FIGURE 5.18c - SIMILAR TO 18a LEVEL 3 POWERED



POST1 STRESS
TEMP

YV=1
DIST=.0116
* XF=.01
* ZF=.0101
SECTION
MX=46.7
MN=18.6
A=20.7
B=23.7
C=26.7
D=29.7
E=32.7
F=35.7
G=38.7
H=41.7
I=44.7

FIGURE 5.18d - SIMILAR TO 18a LEVEL 4 POWERED



POST1 STRESS
TEMP

YV=1
DIST=.0116
* XF=.01
* ZF=.0101
SECTION
MX=38.2
MN=19
A=20.6
B=22.6
C=24.6
D=26.6
E=28.6
F=30.6
G=32.6
H=34.6
I=36.6

FIGURE 5.19

COMPARISON OF FE PREDICTION AND EXPERIMENTAL MEASUREMENT
ALL LEVELS POWERED IN NATURAL CONVECTION

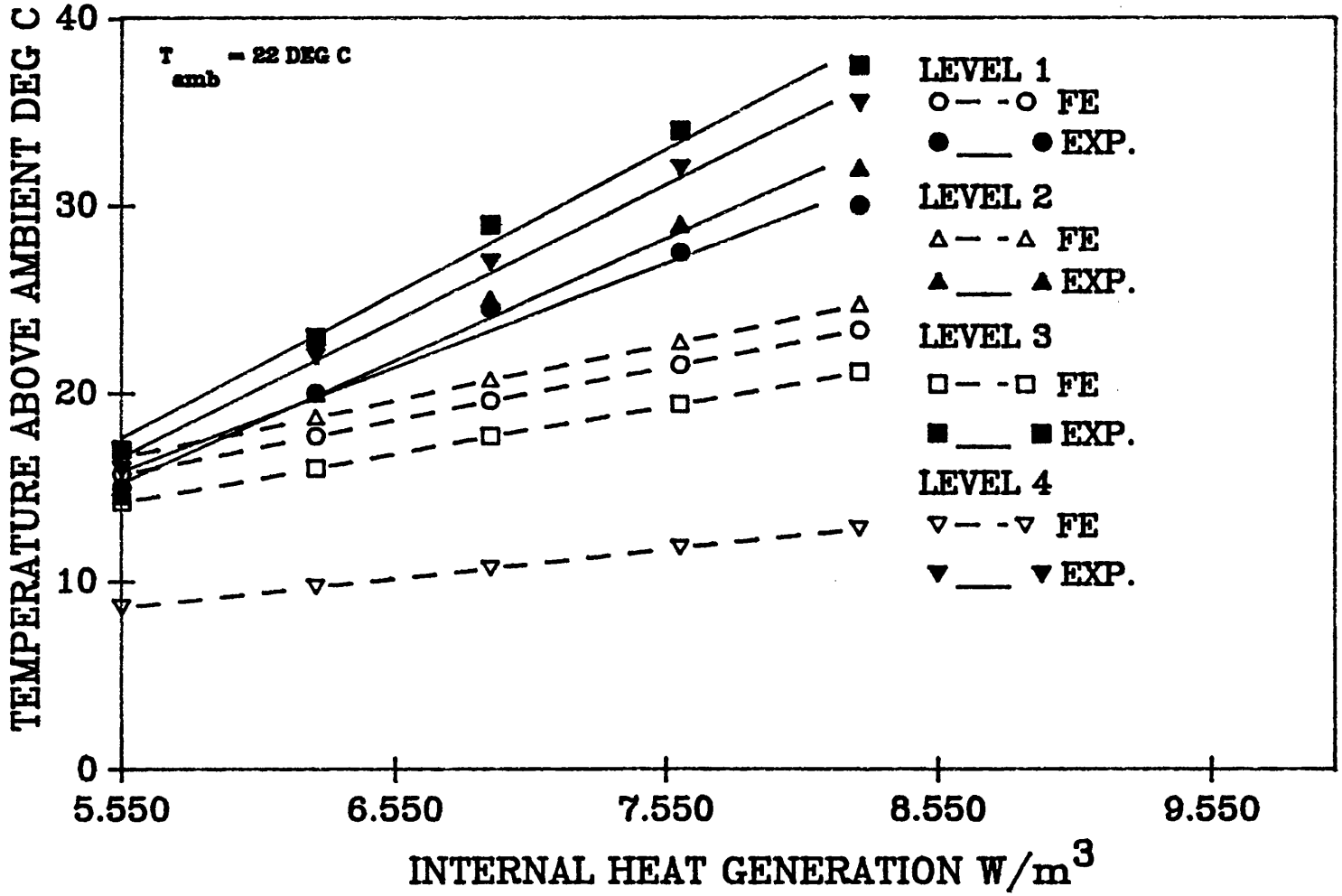


FIGURE 5.20a

TRANSIENT TEMPERATURE RESPONSE REDUCED CONVECTION ALL LEVELS POWERED MARK SPACE RATIO 10%

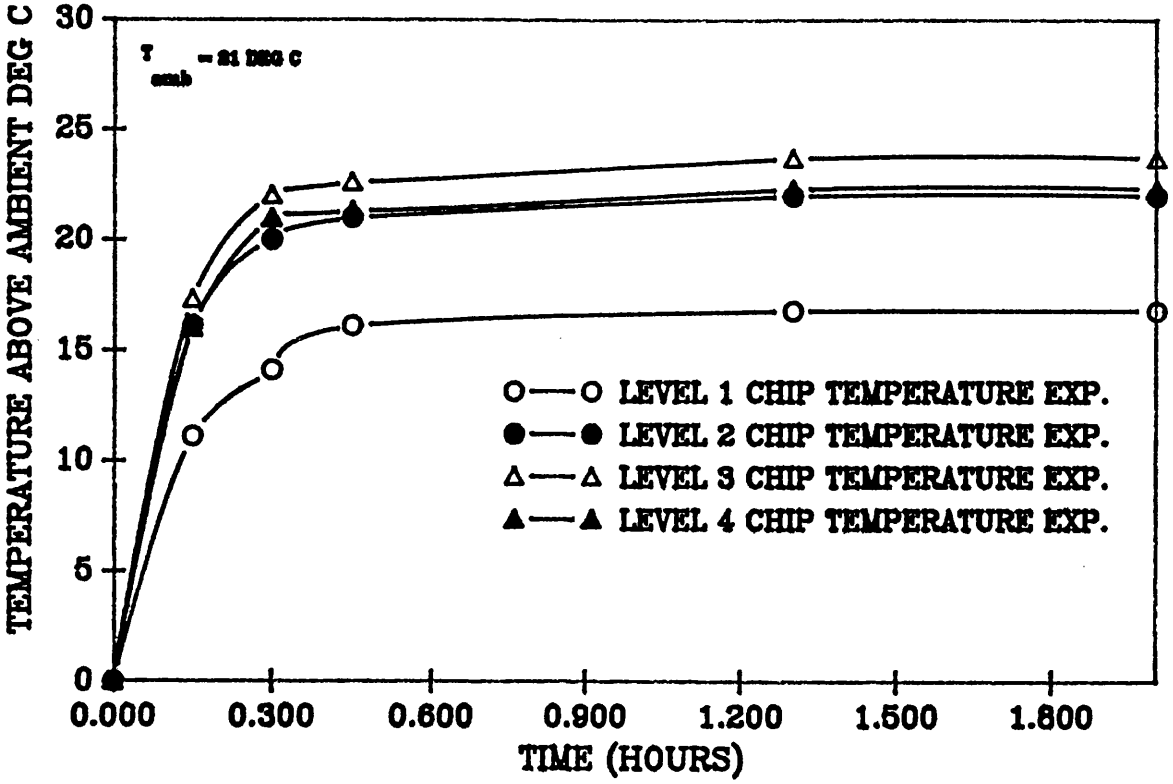


FIGURE 5.20b

TRANSIENT TEMPERATURE RESPONSE REDUCED CONVECTION ALL LEVELS POWERED MARK SPACE RATIO 30%

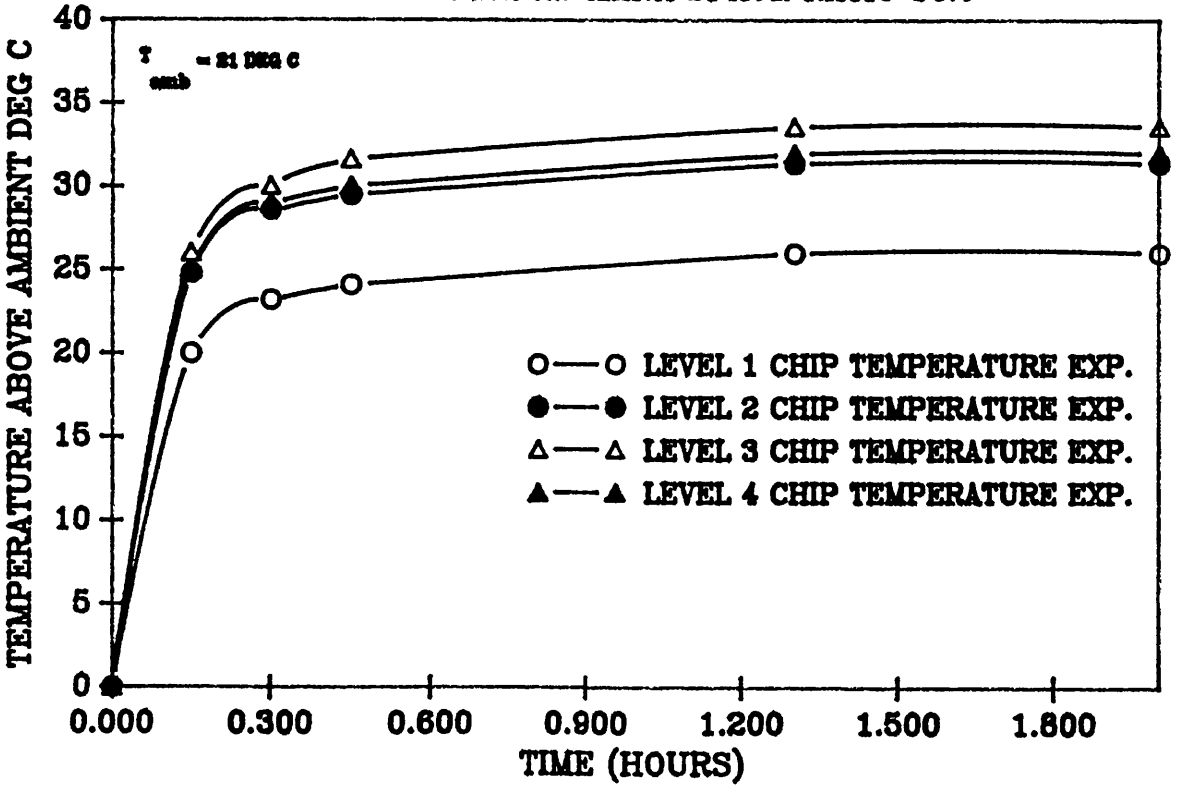


FIGURE 5.21

TRANSIENT FE PREDICTION WITH REDUCED CONVECTION
ALL LEVELS POWERED MARK SPACE RATIO 30%
COMPARED WITH EXPERIMENT FOR LEVEL THREE

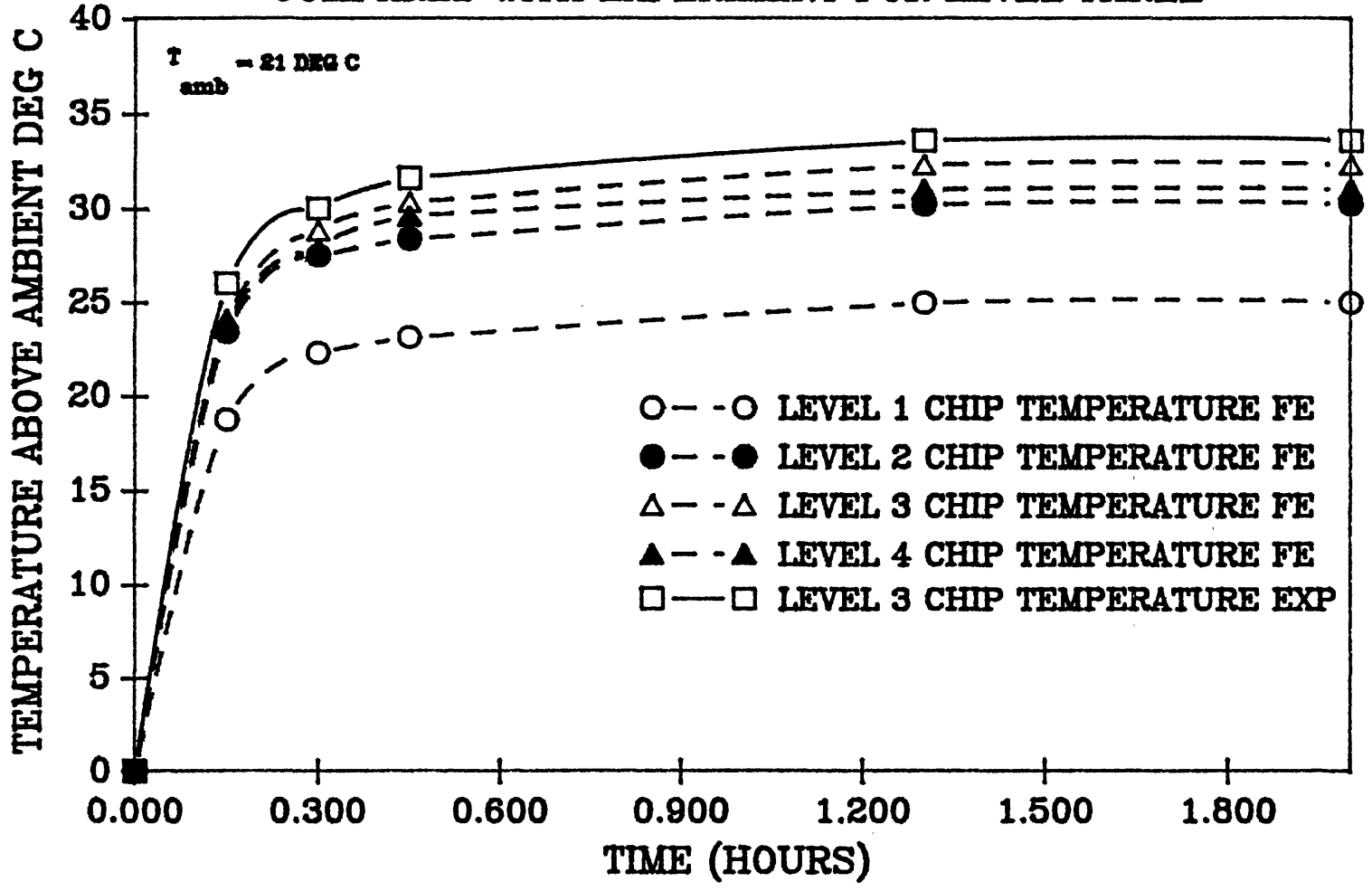


FIGURE 5.22
TRANSIENT TEMPERATURE RESPONSE MOTHERBOARD INSULATED
ALL LEVELS POWERED MARK SPACE RATIO 30%

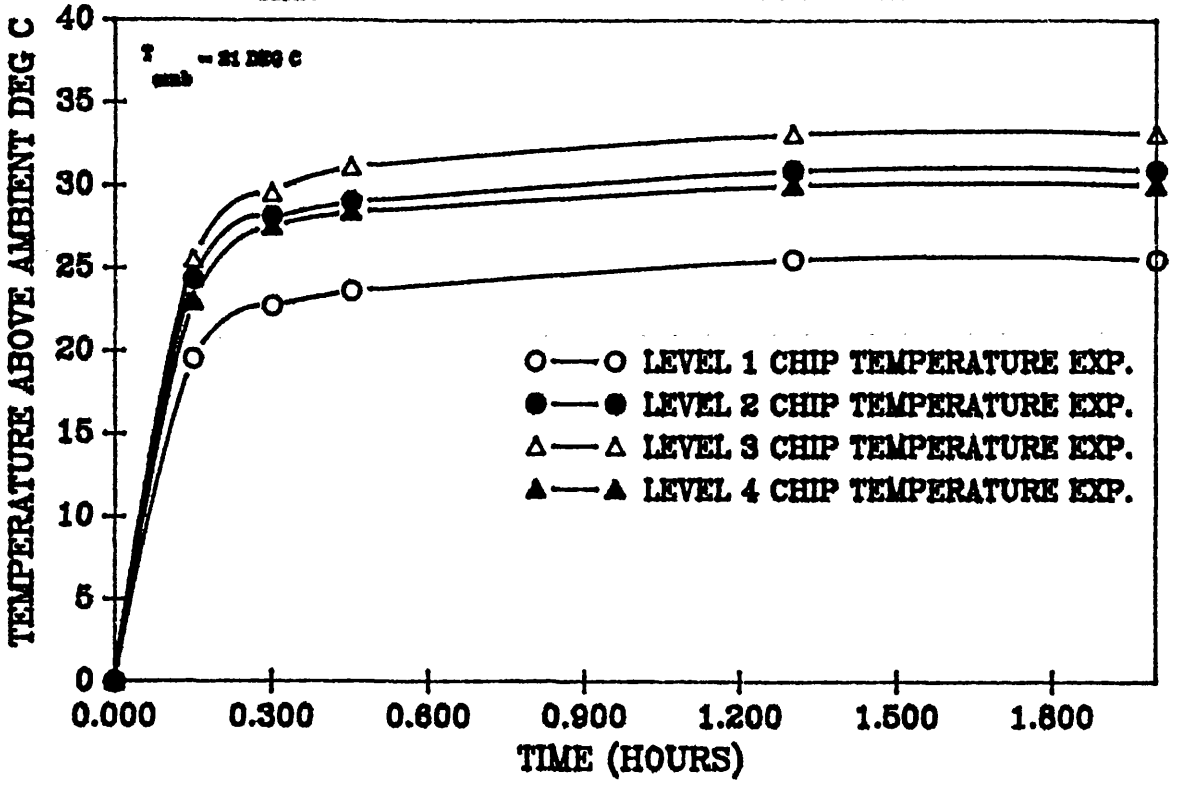


FIGURE 5.23
TRANSIENT TEMPERATURE RESPONSE STACK INSULATED ONLY
ALL LEVELS POWERED MARK SPACE RATIO 30%

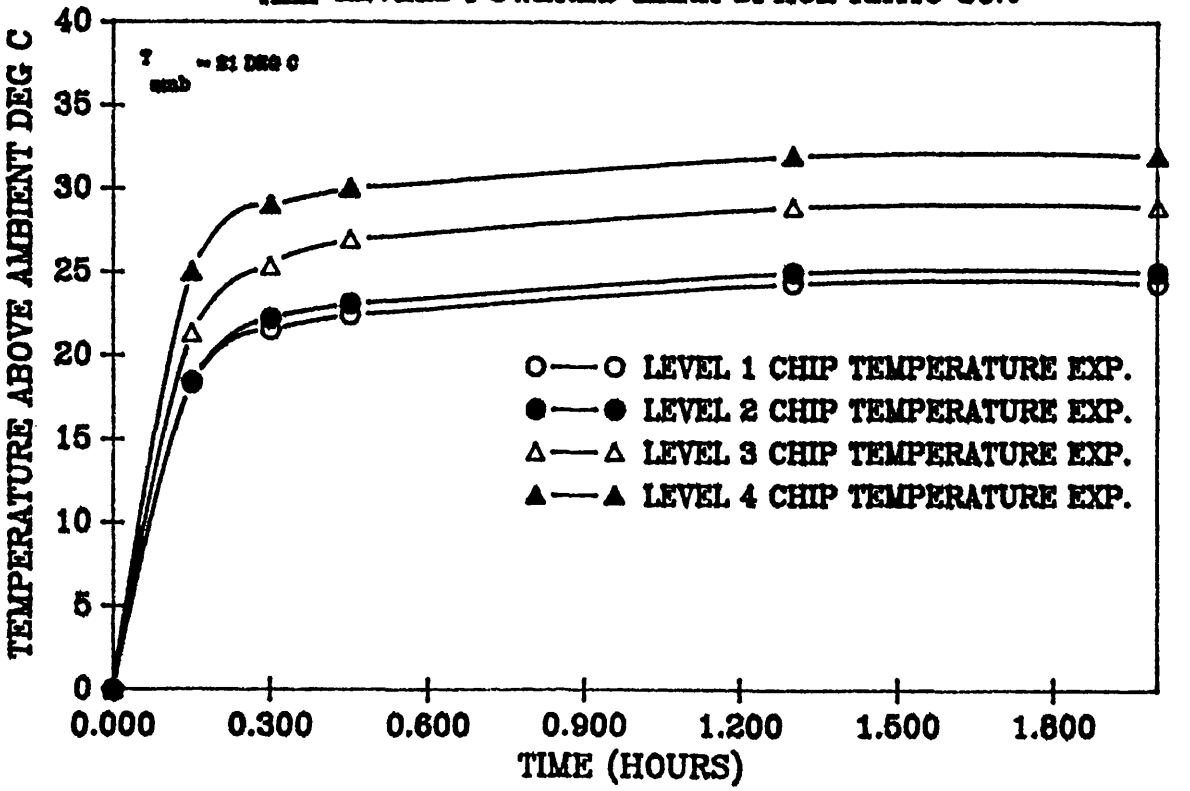


FIGURE 5.24

TRANSIENT TEMPERATURE RESPONSE CHIPRACK IN NATURAL CONVECTION ALL LEVELS POWERED MARK SPACE RATIO 30%

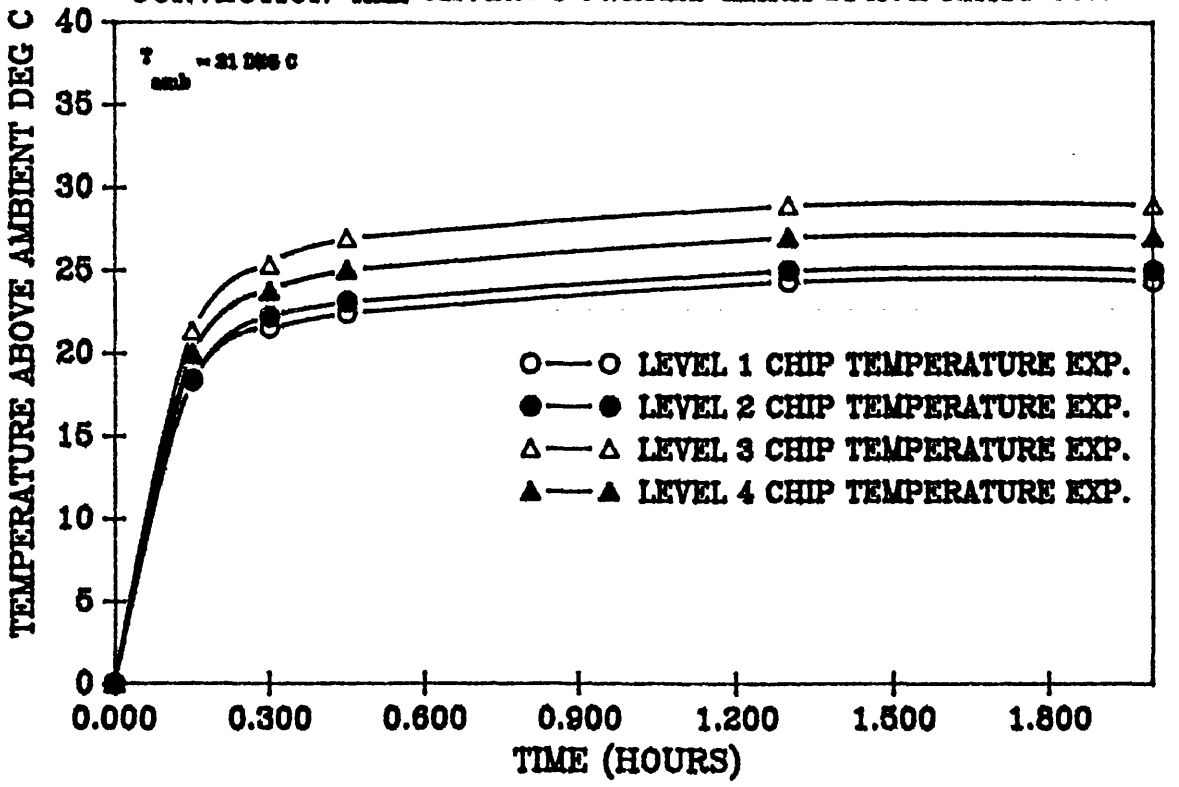


FIGURE 5.25

NORMALIZED TEMPERATURE vs TIME

ALL LEVELS POWERED MS RATIO 30% NATURAL CONVECION

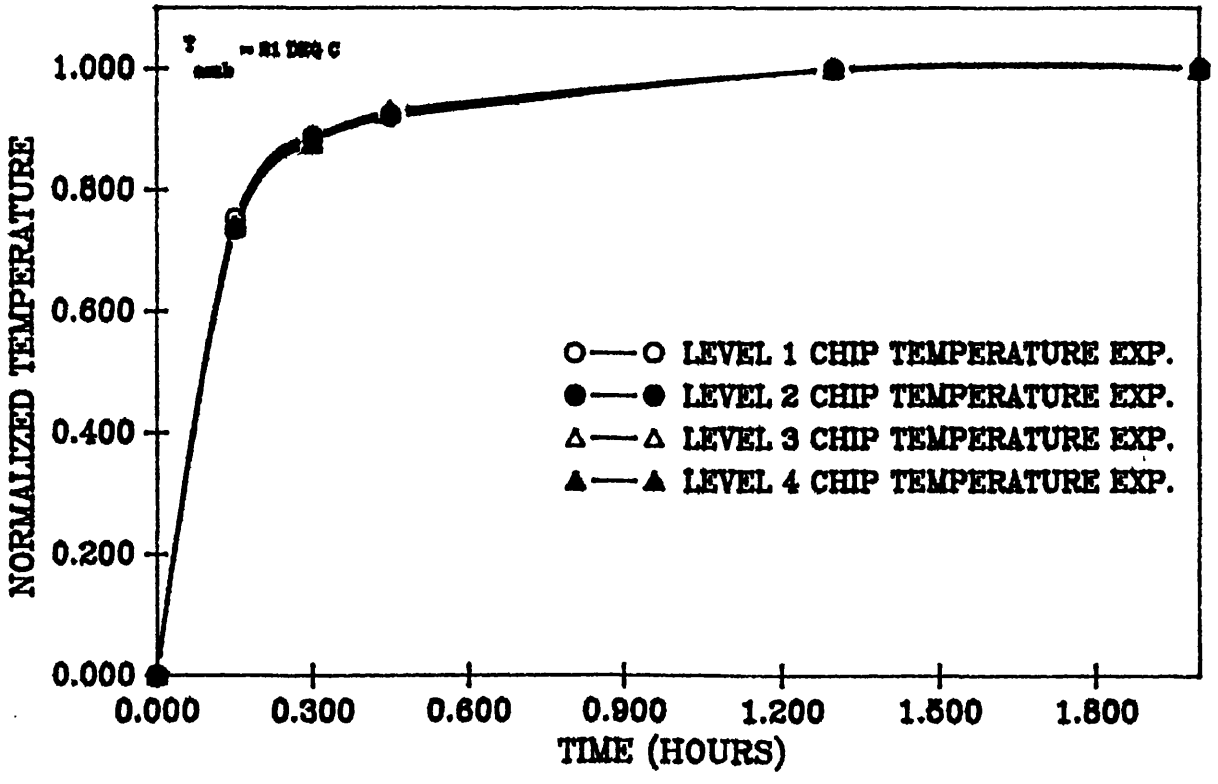


FIGURE 5.26
COMPARISON OF STEADY STATE TEMPERATURE OF THE CHIP
CHIP COVER ON AND OFF

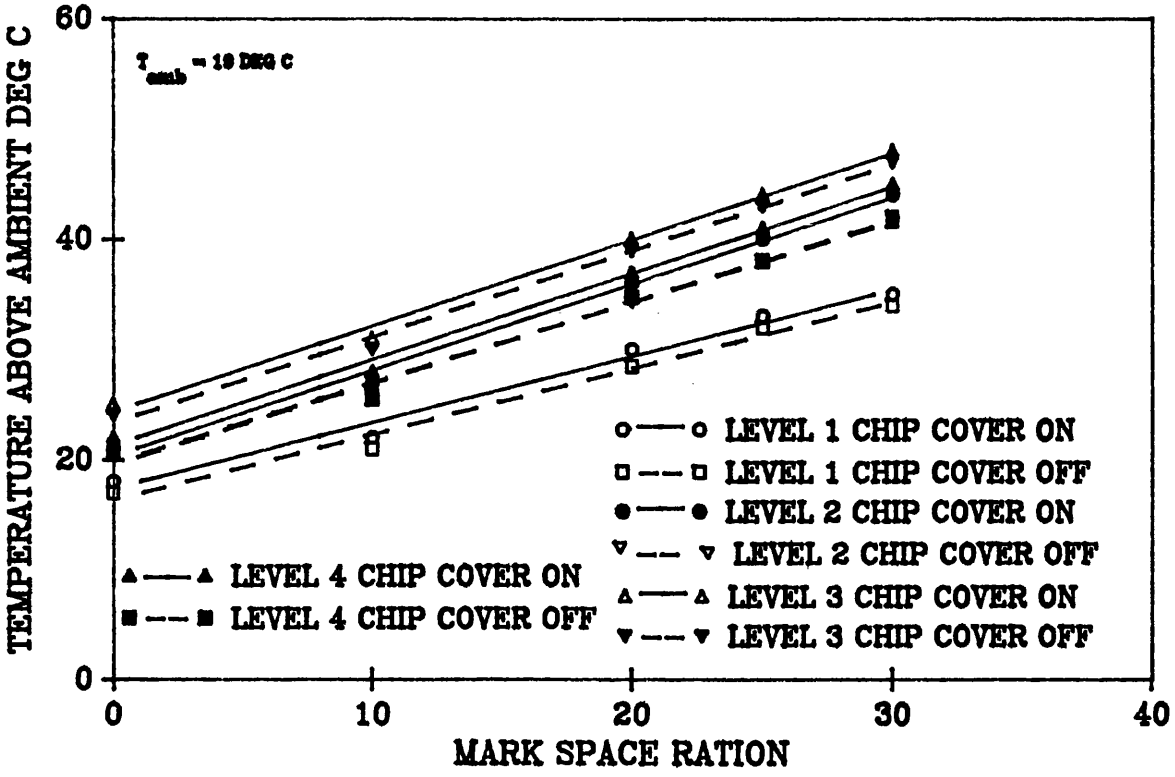


FIGURE 5.27
COMPARISON OF SID AND IR FOR THE FOURTH LEVEL, ALL
LEVELS POWERED IN NATURAL CONVECTION

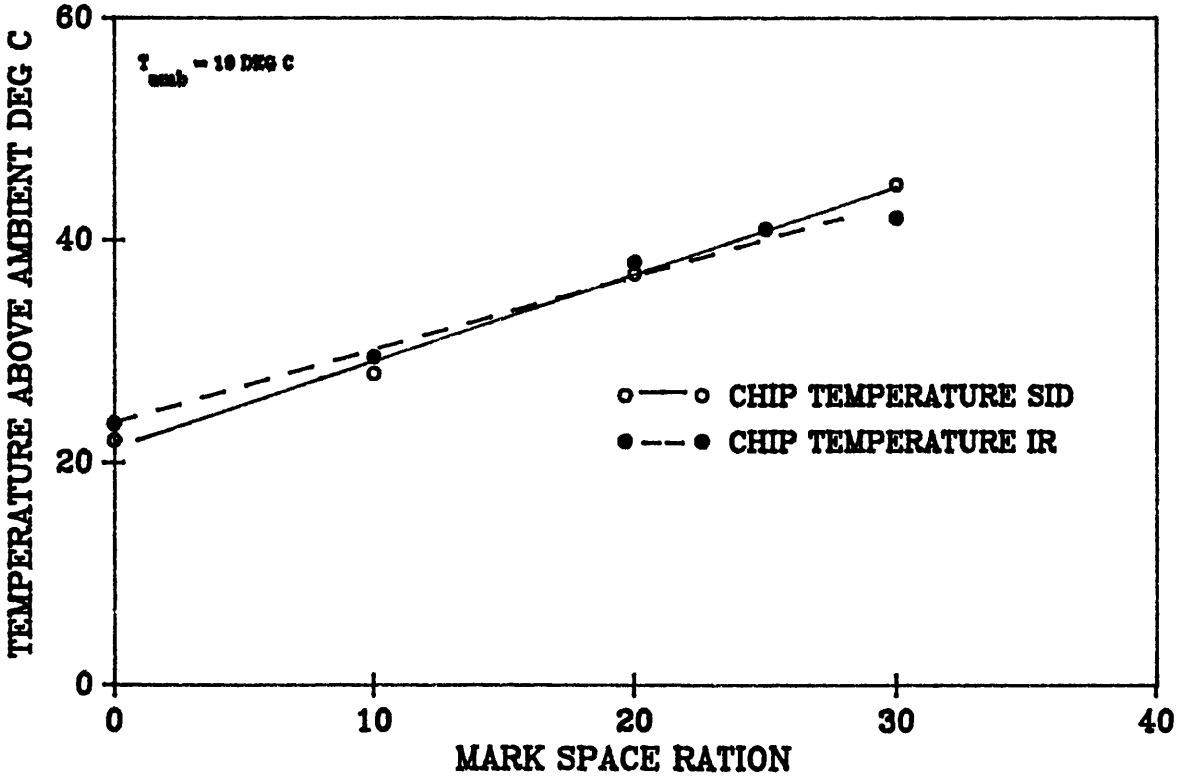


FIGURE 5.28a

LEVEL ONE POWERED IN FORCED CONVECTION

TEMPERATURE vs POWER DISSIPATION

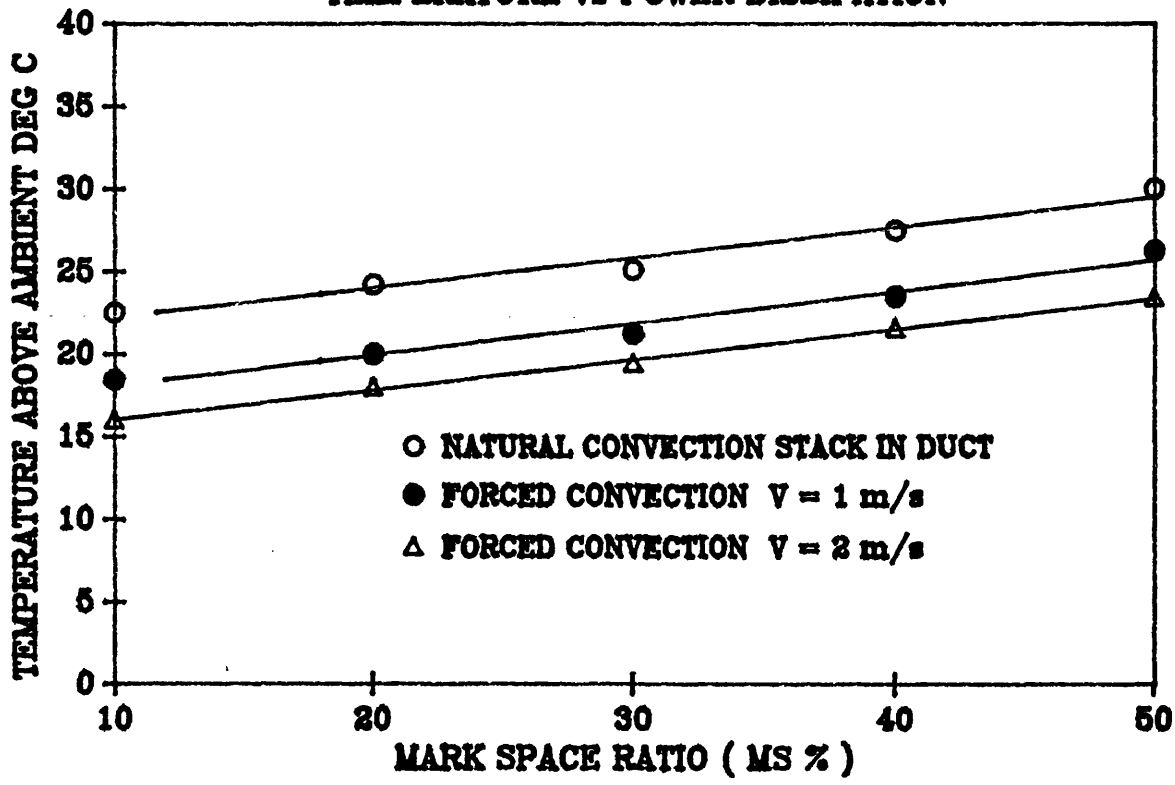


FIGURE 5.28b

LEVEL TWO POWERED IN FORCED CONVECTION

TEMPERATURE vs POWER DISSIPATION

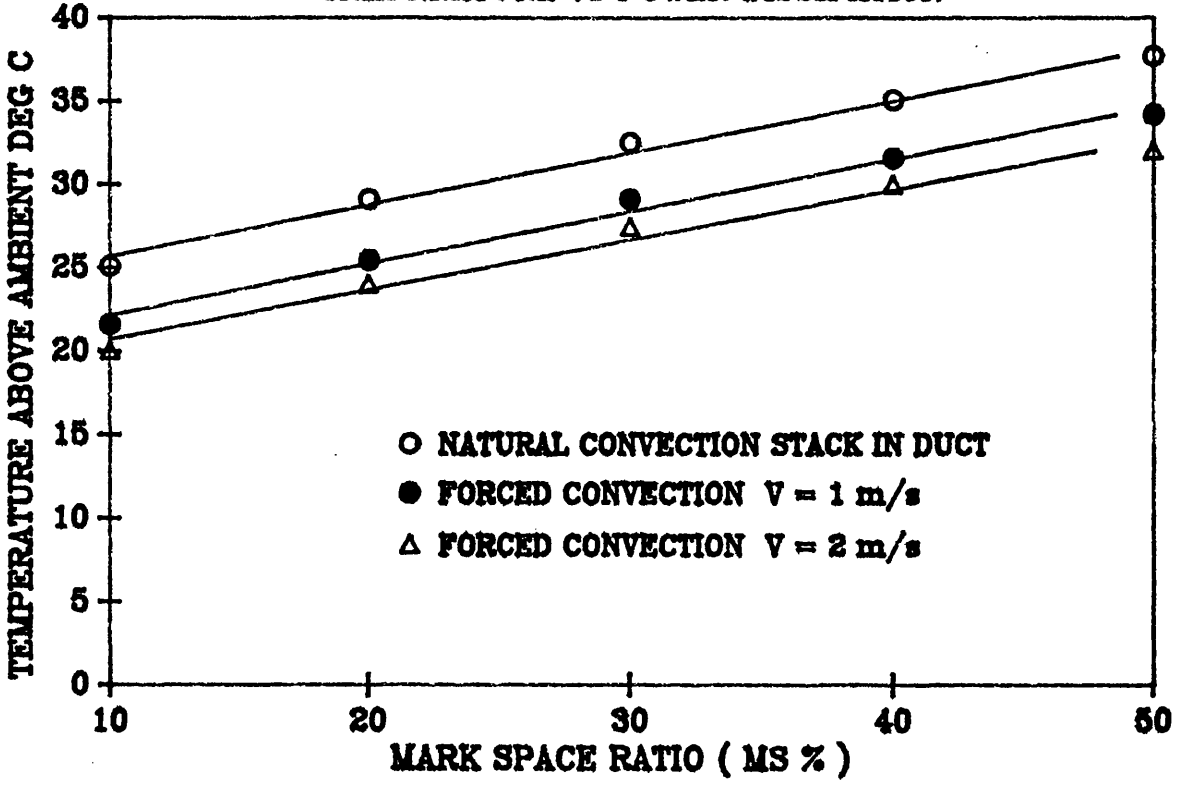


FIGURE 5.28c

LEVEL THREE POWERED IN FORCED CONVECTION

TEMPERATURE vs POWER DISSIPATION

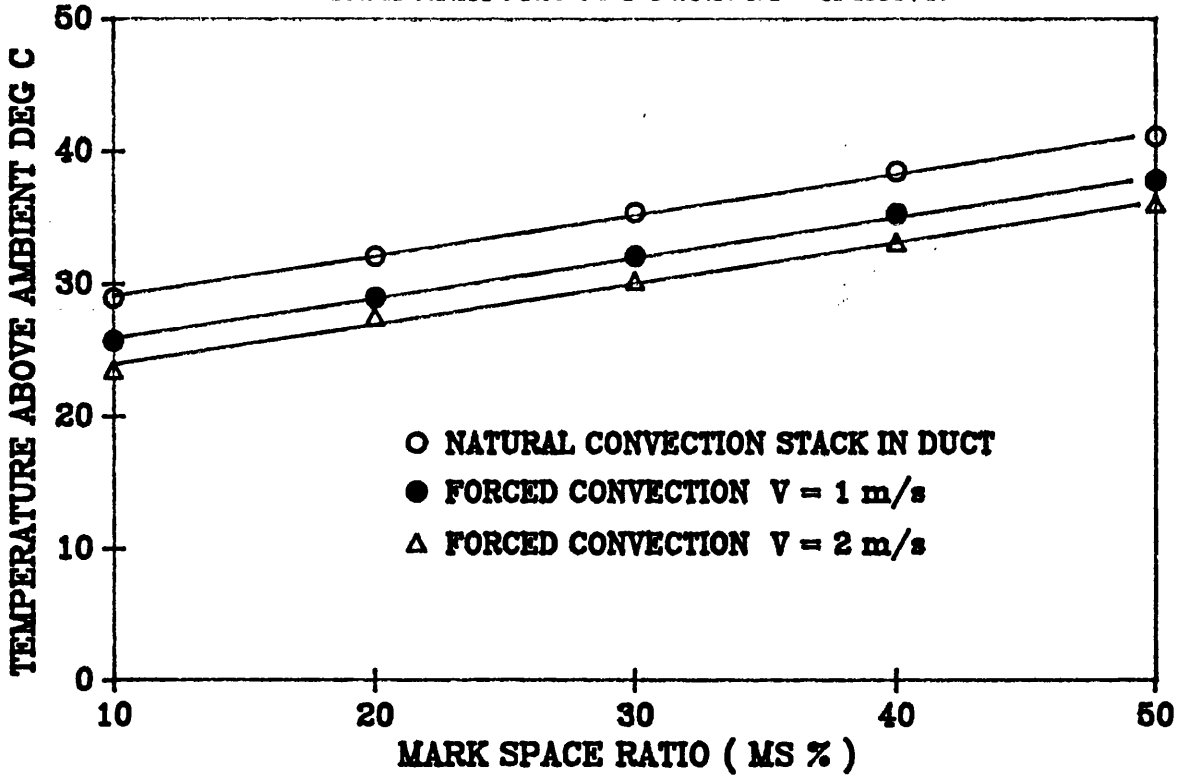
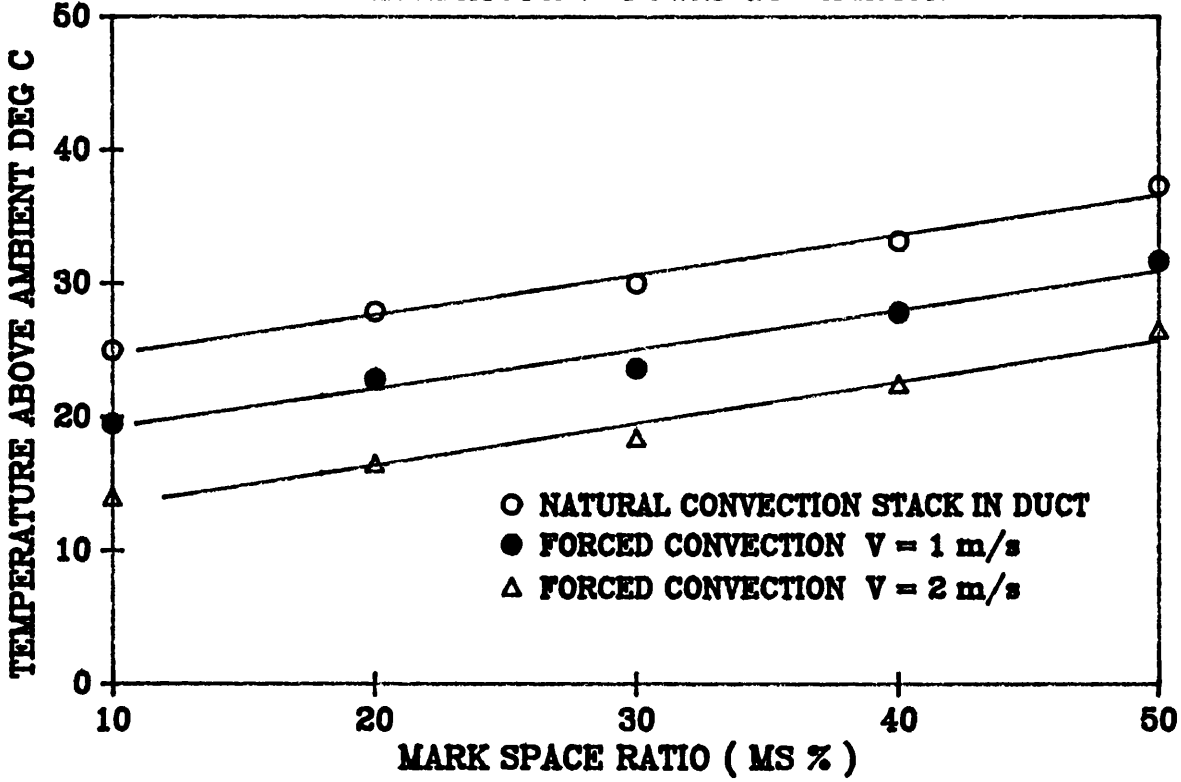


FIGURE 5.28d

LEVEL FOUR POWERED IN FORCED CONVECTION

TEMPERATURE vs POWER DISSIPATION



CHAPTER 6

SURFACE TEMPERATURE MEASUREMENTS AND HEAT TRANSFER PREDICTIONS

6.1 INTRODUCTION

In spite of the fundamental importance of the semiconductor junction temperature as a design parameter, in industrial installations this parameter is seldom known with precision. Difficulties arise because of the complex nature of the air flow conditions, the miniature nature of the electronic modules, and because the conditions of installation frequently depart widely from those used by the manufacturer to specify thermal performance.

The key to the task of making repeatable predictions of the junction temperature is to have a realistic model of the entire thermal transfer process. The conduction path has a complex three-dimensional shape from the module to the substrate. Heat is transferred by convection both directly from the surface of the module, and from the PCB. Manufacturers frequently specify the thermal resistance of an isolated package as a simple fixed value. Such a model is inadequate to represent the true three-dimensional nature of the conduction path from junction-to-case which may change from installation to installation.

In addition, two factors complicate any analysis of the convection process. First, relative to the size of the duct, the modules are large and the separated flow cannot

be characterised as a simple duct flow. Second, the heat transferred from a powered module is transported down the duct in the form of a heated wake flow. Experiment shows that this heated wake does not mix very effectively with the main bulk flow. The calculation is particularly complex in the case when the power is unevenly distributed over a matrix of modules on a PCB. The wake from heated upstream modules raises the temperature even of un-powered modules immediately downstream.

It was realised early in the research that verification of the thermal model required accurate measurements of surface temperature, and that this could most expeditiously be carried out using an infra-red imaging camera. Unfortunately, at the time, the high price of such commercial camera systems put them outside the budget available for this research. To overcome the constraint of finance, a mechanical scanning system was designed and constructed, which moved a normally static IR thermometer, in a raster traverse, over the test assembly. A description of the developments of this system forms the opening sections of this chapter.

The interpretation of the temperature maps from the IR scanner required the construction of realistic FE thermal conduction models. These are described next.

Analysis of the convection process was based on the concept of the thermal wake. This concept and the method of using it are explained in the final sections of this chapter.

6.2 HISTORY AND THEORY OF THERMAL IMAGING

One of the major problems facing physicists during the second half of the nineteenth century was to explain the energy distribution in the spectrum of a thermal radiation. Common experience had shown that objects seem to absorb more or less heat depending on how "dark" or "light" their surface coloration appears to be. Gustav Kirchhoff sought to eliminate this sort of arbitrariness from theoretical considerations by proposing the term black body to describe an object which absorbs all incident radiation energy. In 1860 he introduced his famous law, that a good thermal absorber is also a good radiator.

In 1879, Josef Stefan concluded from experimental measurements that the total amount of energy radiated by a black body is proportional to the fourth power of its absolute temperature, a conclusion which was reached via theoretical thermodynamic relationship by Stefen-Boltzmann in 1884 see equation 3.11. This important relation has since come to be known as the Stefan-Boltzmann law.

During the last decade of the nineteenth century, it became increasingly easy to recognise the basic unity of the different kinds of radiation in the electromagnetic spectrum, but the basic laws of infrared radiation still eluded attempts to derive from them its thermal origin. Many attempts were made to derive the radiation law behind the distribution of radiant energy in the black body spectrum, but even before the end of the century it was becoming clear that it would never be possible to derive a generally valid law from electromagnetic theory alone. It was the German physicist,

Max Plank, who finally recognised that it was necessary to depart from the classical approach. In 1900, he finally produced a derivation of the law of radiation, which bears his name, which precisely describes the spectral distribution of radiation from a black body.

6.2.1 THE INFRA-RED SPECTRUM

The electromagnetic spectrum is divided more-or-less arbitrarily into a number of wavebands distinguished by the methods utilised to produce and detect the radiation. There is no difference between radiation in the different bands, all radiation is governed by the same fundamental laws Figure 6.1.

Thermal imaging makes use of the infra-red spectral band. At the short wavelength end the boundary lies at the limit of visual perception, in the deep red. At the long-wavelength end it merges with the "microwaves" radio wavelength, in the millimetre range.

The infra-red band is commonly further sub-divided into four subsidiary bands, the boundaries of which are also arbitrarily chosen. They include, the near infra-red (0.75 - 3 μm), the middle infra-red (3 - 6 μm), the far infra-red (6 - 15 μm) and the extreme infra-red (15 - 100 μm). Although wavelengths are usually given in "μm" (micrometers), other units are also used. Microns (μ), nanometres (nm), and Angstroms (A). The relationship between these different units are as follows:

$$10{,}000\ \text{A} = 1{,}000\ \text{nm} = 1\ \mu = 1\ \mu\ \text{m}$$

It is possible to obtain an infra-red photograph using infra-red sensitive film loaded into a normal optical camera; this should not be confused with thermal imaging. The distinction is one of the wavelength; conventional infrared film emulsions are sensitive to wavelength no longer than 1.2 μm. The photographic technique does not provide any information regarding temperature distribution over a surface. This is carried out in the longer wavelength usually above the 2 μm to 12 μm band and using a measuring function for temperature evaluation.

6.2.2 NON BLACK EMITTERS

There are three processes which can occur which prevent a real object from acting like a black body: a fraction of the incident radiation α may be absorbed, a fraction ρ may be reflected, and a fraction τ may be transmitted. Since all of these factors are more-or-less temperature dependent, the combination of theses factors are expressed as follows:-

$$\alpha_\lambda + \rho_\lambda + \tau_\lambda = 1 \qquad (6.1)$$

Note: for opaque materials $\tau_\lambda = 0$

Another factor called the emissivity, is required to describe the fraction ε of the radiant emittance of a black body produced by an object at a specific temperature. This is defined as the spectral emissivity ε_λ = the ratio of the spectral radiant power from an object to that from a black body at the same temperature and wave length.

6.3 IR SCANNING SYSTEM

The objective of this part of the research was to design and develop a thermal imaging scanner and incorporate it in the test rig described in chapter 3. It would be used to obtain detailed and accurate surface temperature measurements on the test boards used in the forced convection investigations. The requirements of the mechanical part of the scanning system were as follows:-

1) The system should be capable of scanning a double-eurocard described in chapter 3.

2) The sensing head of a HEIMANN infra-red thermometer (mass 0.8 kg, dimensions 140 x 52 x 52 mm) Figure 6.2 was to be mounted on a mechanical traversing system so that it could scan in a plane.

3) The mounting of the sensing head should be variable vertically to allowing focusing. A 3/8 BSW tripod bush fulfilled this requirement.

4) The maximum allowable time to carry out a raster scan of a double eurocard with steps of 10mm between readings is one hour. The number of point readings is (233/10 x 160/10) $\approx$ 373, the time allowed per reading is therefore (3600/373) $\approx$ 9.7sec (this also includes the time taken to move between the measuring points) with the thermometer set at a response time of 5s the minimum traverse rate is therefore 10/(9.7-5.0) $\approx$ 2.1 mm/sec.

5) Positional accuracy should be better than 2mm in either the x or y directions.

6) The system should be capable of being interfaced with the host computer which would control it.

7) In order to save time and produce a robust design, standard parts were used wherever possible. Specialised parts were kept simple for the same reason.

8) Initially, the scanner was designed to operate in a horizontal plane. However later operation might be in a vertical plane.

9) A prototype design was to be used for feasibility studies.

6.4 EXPERIMENTAL METHOD DESIGN CONSIDERATIONS

Initially the design in Figure 6.3 was considered. The sensing head was mounted on a steel platform driven by two stepper motors via lead screws in X and Y direction although this was successful with relatively good accuracy, it was an unacceptable design because of the time taken by the lead screws to move the sensing head to its destination.

A new design was considered using toothed belt drive. The belts are driven by two stepper motors, one mounted on the outer frame and the other on the inner frame Figure 6.4. The inner and the outer frames are supported by a slider blocks which have drilled through holes fitted with Oilite bushes at each end. The slider blocks run on slider bars. The latter design proved positive, both for the accuracy and speed of the scanner Figures 6.5 - 6.7.

6.4.1 STEPPER MOTOR TORQUE REQUIREMENT

In the calculation of the load on the stepper motors, the coefficient of friction f for the slider blocks was assumed to be 0.2, a typical value for metal sliding on metal without lubrication [73].

i) In the Y-direction

The weight of the sensing head was 7.85 N. with an additional 1 N for the weight of the mounting plate. The force required was 1.77 N with a friction factor of 0.2. Additional friction in the two pulleys was estimated assuming a belt tension of 10 N.

The total force required in the Y-direction is therefore 5.77 N.

ii) In the X-direction

Assuming the mass of the inner frame less the mounting plate to be 300 g. The weight of the inner frame was estimated as 11.8 N. With the two pulleys, and a friction factor of 0.2, the motor load required was 6.4 N.

6.4.2 SPECIFICATION OF THE STEPPER MOTORS SELECTED

i) TORQUE

The stepper motors selected were cheap, light weight; a number of different gearboxes were available to fit them if required. With pulleys of nominal diameter 19.9 mm, the maximum possible load can be calculated as follows:-

$$LOAD = \frac{(R \times T_m)}{r} \qquad (6.2)$$

where:

R = Gearbox ratio
T_m = Maximum working torque of the motor, m
r = Drive pulley radius, m

ii) TRAVERSE SPEED

The chosen stepper motors had a pulse rate of 62.5 steps/sec. The traverse speed can therefore be calculated as follows:-

$$TRAVERSE\ SPEED = \left(\frac{r \cdot p \cdot i}{R}\right)\left(\frac{\pi}{180}\right) \qquad (6.3)$$

where:-

r = Drive pulley radius, 9.945 mm
P = Pulse rate of the stepper motor (Steps/sec)
i = Motor step angle (1.8 Degrees for the selected motors)

6.5 OVERVIEW OF THE MECHANICAL DRIVE SYSTEM

The IR sensing head mounting plate is moved by a stepper motor attached to the inner frame. The motor drives the mounting plate via two toothed belts passing over two drive pulleys on a common shaft which is coupled to the stepper motor. The drive belts pass over two identical idler pulleys on the other end, which allow adjustment to vary the belts tension. The ends of the belts are brought together and clamped onto the slider blocks which also house the two limit switches in the Y-direction Figure 6.7.

A similar arrangement was used to provide the traverse in the X-direction. The pulleys and motor being mounted on the aluminium angle sections, with belt and limit switches clamps on the inner frame end plates. This design was chosen so that the sensing head could be moved to any location. The use of two drive belts in any direction was to eliminate any possible twisting of the frames and sensing head mounting plate. The purpose of the limit switches was to prevent the thermometer mounting plate from over running its designed range and also to provide a reference "home" position for the scanner.

In order to keep the weight of the scanner to a minimum, aluminium sections were used whenever possible. However to overcome vibration problems, one part of the scanner was manufactured from steel.

6.6 CONTROLLING THE MECHANICAL SCANNER

6.6.1 HARDWARE REQUIREMENTS

The hardware requirements consists of an Autonomous Data Acquisition Unit (ADU) (the Mowlem described in chapter 3), a host computer, stepper motors and its electronic driver cards, limit switches and power supply, see Figure 6.8. The computer is used to input a "scan schedule" via the software, which defines the matrix to be scanned on the target surface. This grid is then converted into a number of steps and a direction, which are then relayed to the Mowlem unit. The Motor Control Interface (MCI) card in the Mowlem converts the number of steps into pulses which are then sent to the motor driver cards. The direction is converted into a high or low voltage level at the MCI output. The motor driver card drives the stepper motor coils in sequence until it stops receiving pulses at its input. The limit switches are set on X to stop the pulsing if the scan schedule is out of range. The Power is supplied individually to each stepper motor and its associated motor driver card individually by a DC power supply. The driver card has a 12 Volt regulated output which is used to power the Mowlem MCI card.

The precision of the mechanical Scanner is limited, on the software side, to that of the ADU precision. Some details are listed below; for further details reference should be made to the ADU manual.

The Analog Input Module (AIM) which converts the analog signal from the thermometer output into a digital signal for recognition by the computer has a variable gain. For the XY-scanner this is set at gain 3 ranging from (-1.25V to 1.25V) to match

the thermometer output range (0 to 1V). The digital signal has 12 bits, which dictates a precision of:-

$$1 \text{ bit} = (2 \times 10) \times 2^{-3} / 212 \text{ Volt} \approx 0.6 \text{ mV}$$

i.e: 1 bit ≈ 0.06 °C (thermometer measuring range set at 0 to 100°C)

Greater precision can be obtained by means of an offset, and by using the negative part of the range mentioned above. However this is not really necessary, because the ADU reads from its AIM channels every second and the thermometer requires at least two second time delay between each reading, (thermometer response time).

6.6.2 CHARACTERISTICS OF THE INFRA-RED THERMOMETER

The temperature sensing device used in this part of the research is the " **Heimann KT16** " infra-red thermometer. In this section only those output characteristics of the thermometer are described which are relevant to the control system, for more details reference should be made to the manufacturers manual. The thermometer output response from the analog terminal is non-linear. Figure 6.9 illustrates the output voltage sent to the ADU as a function of temperature. After the AIM has converted this analog signal into a digital format, the voltage is calculated by the computer according to the preset AIM gain.

A set of ten points which characterise the curve of Figure 6.9 has been chosen and stored in the computer memory Table 6.1, (giving the temperature every tenth of a volt). The unknown temperature is estimated by linear interpolation between the two

nearest sampling points as illustrated in the example below.

Volt	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.9	1.0
T °C	15.1	28.1	39.9	50.5	60.2	77.5	85.5	92.9	100

Table 6.1 - The sampling points from Figure 6.9 for linear interpolation.

For example, for a voltage of 0.361V the temperature is evaluated as follows:-

$$T + 39.9 + 0.061 \times (50.5 - 39.9)/0.1 = 46.37\ ^{\circ}C$$

6.6.3 SOFTWARE REQUIREMENTS

The controlling loop of the XY-scanner is completed by a module called "SCAN".

This program is an essential part of this design and has two main aims:-

(a) Driving the stepper motors.
(b) Collecting data from the thermometer.

These aims must be coordinated to form a coherent scanning sequence. The sequence consists of a square matrix, and the parameters capable of variation by user are as follows:-

i) The scanning step length (the precision of the scanning)
ii) The start and finish coordinates of the scan in the X and Y direction.
iii) The infra-red thermometer response time, (this will affect the duration of scan).

During a scan schedule the software monitors and displays the following:-

i) The current location of the infra-red sensor.
ii) The temperature of the target at that location.

When scanning is completed a message is displayed informing the user of the final destination, before returning to home position.

6.6.4 GENERAL ALGORITHM OF THE SCAN PROGRAM

The algorithm which forms the basis of the scan program can be generally described

as follows:

[INITIALISATION]

(a) - declare serial port for communication with ADU.
(b) - reset ADU.
(c) - set ADU channel for Analog to Digital conversion of thermometer signal.
(d) - initialise thermometer calibration curve.

[STARTING UP]

(a) - drive the camera to home position or check the home position.
(b) - check limit switches status.

[SCAN SCHEDULE DEFINITION]

(a) - input scanning parameters.
(b) - evaluate number of motor steps per scanning step length.
(c) - evaluate dimension of temperature distribution array.

[SCANNING]

(a) - calculate displacement to next scanning point.
(b) - drive both motors.
(c) - update camera position.
(d) - check that the drive motors have stopped, and check limit switches status.
(e) - wait (thermometer response time).
(f) - take a reading, convert it into a temperature and store it.
(g) - display information for user.
(h) - loop until scanning completed.

[DATA PROCESSING]

(a) - save the temperature distribution on disk (the file format is {n,m,T[0,0],T[0,1],....,T[0,m],T[1,1],.....,T[n,m]})

[END OR LOOP]

(a) - Drive the sensing head to home position, and close the channel.
(b) - END

6.7 IMAGE PROCESSING PROGRAM

With this design the temperature of an scanned object is measured at a finite number of discrete points. The size of the temperature data array produced from the direction is dependant on the raster scan step size and the area scanned. In addition the data were to be displayed on the same computer which controlled the scan, VDU size (EGA 500 x 200), thus the infra-red image required to be scaled in both X and Y direction to match the screen size.

In order to achieve an IR image which could easily be interpreted, a pallet of 14 colours was chosen. As suggested by [73], putting the colour in an order of brightness rather than wavelength seems best suited to the characteristics of the human eye. Each colour represents one fourteenth of the temperature range scanned. By this technique a colour thermal image was produced from the array of the scanned temperatures. To carry out the analysis of each map with the image program, after loading the data the computer displays a menu on the screen Figure 6.10 a-c.

6.7.1 IMAGE SCALING PAINTING AND INTERPOLATION TECHNIQUES

Two methods of producing the thermal image on the display unit, were considered "painting" and "interpolation".

(i) PAINTING

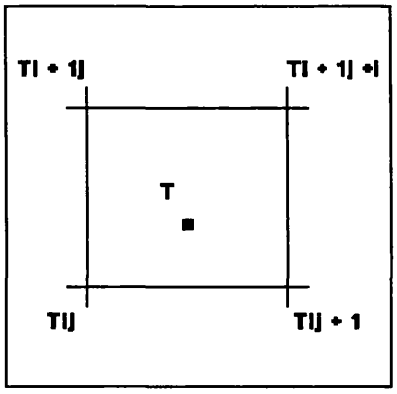
This technique requires two stages. Firstly a contour map is generated. Then the areas between the contour lines are PAINTED with the right colour. The contour map is

simply a drawing of several isothermals. The way it is produced is not difficult in principle, but can sometimes result in an error when two isothermals become too close to each other, or when the curvature of a single isothermal becomes very small in some region. Because of these difficulties the painting technique was rejected and the interpolation technique was adopted.

(ii) LINEAR INTERPOLATION

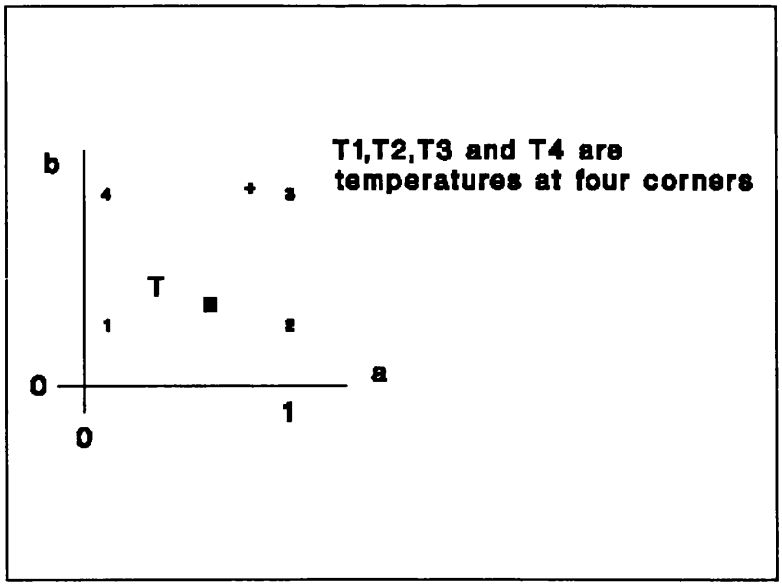
Is based on the principle that the temperature at a certain point may be deduced by mathematical interpolation between temperature values in the immediate vicinity of that point. An interpolation is a function which values at a given set of points are imposed, and which is built as a linear combination of functions out of a chosen complete or incomplete basis).

In order to scale up the infra-red temperature points to fill the available graphics screen two methods were adopted. One option of the image program uses the fourth order interpolation, to compute the immediate surroundings temperature of a scanned point in a square format as shown below:-



Given a point X of coordinates (x,y) in the main coordinate system (attached to the board), defining its local coordinates as (a,b) in a local coordinate system attached to

the interpolation square.



We have a polynomial interpolation out of the quadratic generating set (1,a,b,ab,a^2,b^2) which is reduce to four elements in the form:-

$$T = [\ 1\ a\ b\ ab\ ]\ [\ \underline{P}\ ]\ \{T_i\} \qquad (6.4)$$

Where:

i = 1 - 4
P = The square matrix

Hence the expressions for the temperatures at each of the four nodes of the square element is given by:-

$$T_1 = [\ 1\ 0\ 0\ 0\ ]\ P\ \{\ T_i\ \}$$

$$T_2 = [\ 1\ 1\ 0\ 0\ ]\ P\ \{\ T_i\ \}$$

$$T_3 = [\ 1\ 1\ 1\ 1\ ]\ P\ \{\ T_i\ \}$$

$$T_4 = [\ 1\ 0\ 1\ 0\ ]\ P\ \{\ T_i\ \}$$

Therefore:

$$P = \begin{matrix} 1 & 0 & 0 & 0^{-1} \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 \end{matrix} = \begin{matrix} 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ -1 & 0 & 0 & 1 \\ 1 & -1 & 1 & -1 \end{matrix} \qquad (6.5)$$

Hence, substituting in equation 6.4 gives:

$$T = (1-a)\,(1-b)\,T_1 + a(1-b)\,T_2 + abT_3 + b(1-a)\,T_4 \qquad (6.6)$$

The thermal image can now be generated reading the temperature array file as follows:-

i) scan every pixel of the image

ii) determine the square in which the current pixel lies

iii) find the temperature of the corresponding point equation 6.6, and thus the temperature and then

iv) plot the temperature and then loop for all pixel.

An IBM-AT (with a 286 processor) takes about 5min to plot an image in a (500x200) frame. This is acceptable when compared to a scan time of half an hour to scan a double euro-card.

Difficulties may arise with the above method when the temperature variation between the four infra-red temperatures points is not linear. This may occur if a chip/board boundary is crossed by the four points. Since the package is several degrees hotter than the surrounding board a step change in temperature occurs around its border. Thus the temperatures calculated for the display are not correct at the chip boundaries.

Here the steps in temperature on the board itself are smoothed out by the interpolation algorithm for the image on the screen.

In order to avoid the inherent difficulties with interpolation, an option of switching off the interpolation was introduced into the program. The software then merely expands one temperature point to occupy six by three pixel on the display unit, effectively reducing the resolution of the graphics to that of the raster scan Figure 6.10d illustrates a typical thermal image of the Euro-card in natural convection with interpolation off.

6.7.2 "X" AND "Y" DIRECTION TEMPERATURE RISE INDICATORS

As an aid when scanning the temperature of the entire PCB, an option was introduced to indicate the continuous temperature rise along the PCB, based on the temperature of the raster plot and the position of the packages on the PCB. The temperature rise was plotted over a black and white vertically striped background, where the black indicated the position of the package and the white indicates the board area exposed during the scan. Fourteen horizontal stripes indicate the temperature scale and each strip is then colour coded according to the colour range scale. The numerical values of these points can be printed out if required Figure 6.10e-f.

6.7.3 TEMPERATURE PROBE CURSOR

To facilitate monitoring of the individual pixel temperatures on the raster plot, a moving cursor control was introduced. The cursor appears in the centre of the screen as soon as the image is completely plotted. This cursor can be moved to any location on the screen using the control caricatures ("l" [left] - "r" [right] "t" [top] "b" bottom) where the coordinates and temperature of that point is displayed on the right hand side of the screen under the colour scale. This facility is particularly useful when comparison with FE is required.

6.7.4 TEMPERATURE SCALE CONTROL

The range of the colour scale on the raster plot, by default, was based on the maximum and minimum temperatures available within the scanned area. To enable closer analysis of the raster plot an option was introduced which allowed the selection of a predefined temperature sub-range of the colour scale introduced. This was particularly useful when it was coupled with the zooming window for enlargement of an arbitrary area on the raster plot. Moving the cursor to any location and typing "q" will indicate one limit of the zooming window, whilst the diagonally opposite corner selects the other limit of the zooming window, then an automatic relief map of the selected window is plotted. Another option allows selection either of an absolute temperature plot or of the temperature rise above ambient Figure 6.11d.

6.7.5 3-D COLOUR MAP PRESENTATION

This format of presentation was introduced to provide a better visual understanding of the temperature distribution of the scanned area. With this method the raster plot is displayed in the form of a three dimensional isometric image using a cartesian coordinate system. Temperature is plotted in the "z" direction (vertically up wards), and is colour coded in the same fashion as the raster plot. The X and Y coordinates of the scanned area are plotted on the horizontal and diagonal respectively. The visual presentation of the temperature distribution in this format enables quick estimate of hot spots.

6.8 TESTING THE COMPLETED SYSTEM

Before the scanner was incorporated into the test rig described in chapter 3, several tests were carried out to establish its accuracy.

A 100 mm^2 matrix of 2 mm diameter circles was drawn on an A4 sheet in steps of 10 mm centres. The sensing head was mounted in its slot on the mounting plate, with the (80 mm long 2 mm diameter) target focusing gauge placed on the detector. The A4 paper was adjusted relative and parallel to the scanning plane, such that the gauge 2 mm area covered one of the corner circles. A scan schedule of 100mm x 100mm in steps of 10mm with thermometer delay time of three minutes was issued. The intermediate locations reached during the scan was marked on the A4 sheet and measured. The scanning accuracy was found to be within acceptable limits of

± 0.3 mm Figure 6.11a. The image processing software was tested using a temperature array file of a double Euro-card described in chapter 3 in natural convection, Figure 6.11b illustrates the thermal image with interpolation option selected.

To establish the suitability of the system as applied to objects other than a PCB the back of a human hand was scanned, as illustrated in Figure 6.11c. For this test the three fingers to the left of the image were folded to test its resolution. Analysis of this image further illustrates that the base board acted as a heat sink.

6.8.1 OUTLINE OF CHIP POSITION SUPERIMPOSED

When scanning the double Euro-card in some of the raster plots it was difficult to ascertain the exact position of individual packages. To overcome this problem an option was built into the image processing software to highlight the outline of the packages on to the raster plot Figure 6.11d.

6.9 INCORPORATING AND TESTING THE SYSTEM IN A TEST RIG

In order to get a complete temperature map of the double-Euro card, the mechanical scanner was incorporated into the research rig described in chapter 3, Figure 6.12a. However before any tests could be carried out the PCB housed in the perspex test section had to be made thermally transparent to the sensing head through the perspex duct wall. This involved a search for a suitable window material and subsequent design. A variety of window materials was tested as potential window material,

Appendix 3. Of these PROPAFILM "C" was chosen, because its absorbtion of IR is quite small. Also it had reasonable resistance to stretching and yielding at the expected operating temperatures.

However the use of the propafilm C meant that compensation was required for the temperatures detected by the infra-red thermometer due to absorption in the window. After experimentation (see Appendix 3) it was found that the relationship between the actual temperature and the IR detected temperature through the film was not linear. A correction factor for absorption was sought in the form:-

$$\textit{CORRECTION FACTOR} = \frac{\textit{(IR TEMP. DETECTED - ACTUAL TEMP.)}}{\textit{IR TEMP. DETECTED}}$$

The value of the correction factor varied by no more than 10% up to an IR temperature of 70° C, but above this the correction increased somewhat. To overcome this problem, and to provide accurate corrections over the entire operating temperature range, values of the difference (IR detected temp. - actual temp.) were stored as a data base at three degrees increments in IR detected temperature.

The corrected temperature was then obtained by interpolation in this stored table of values. This module was then added to the image program as an option. Having overcome the absorption problem, a layer of propafilm C was then stretched and secured by a coarse mesh of fine nylon fishing line this virtually eliminated any possible sagging of the film in high velocity tests Figure 6.12b. The mesh is out of focusing range of the infra-red sensing head hence, the effect on image could be

neglected.

As a datum for the emissivity of the PCB a small section of the PCB was painted mat black. Temperatures measurements were carried out on both the painted and non-painted areas. It was found that the board behaved almost as a black body. However setting the instrument emissivity to a value of 0.97 avoided painting the board completely black.

With the new configuration of the test rig, a series of tests was carried out with all chips on the PCB powered uniformly, 1.2 W/chip. Air velocities of 2.5, 3.5 and 5 m/s were employed to provide forced convection cooling. Once steady-state conditions were established (normally taking 30 minutes) the scan program was activated to produce the temperature array file required by the image program for later analysis. At the same time the thermistor readings were recorded. Temperatures on the under side of the board were also recorded for comparison.

6.10 PRESENTATION AND DISCUSSION OF RESULTS COMPARISON OF THERMISTOR AND IR TEMPERATURES

6.10.1 UNIFORM POWERING

Figures 6.13a to 6.13c show typical thermal images of the PCB for the power and the velocity range mentioned above. The surface temperatures of the packages from these images were compared with those recorded from the thermistors (described in Chapter 3).

In each case the chipoverlay option was activated. The diagonals across the overlay were drawn to reveal the exact position of the centre pixel on the top surface. Relative to this position, the thermistor is positioned directly opposite on the under surface of the package (see Chapter 3). The cursor was then moved to this point and the temperature was recorded. Figures 6.14a, 6.14b and 6.14c show the comparison of the IR and thermistor temperatures.

Although the general trend from the two temperatures are similar the IR temperatures are higher than the corresponding temperatures measured by the thermistors. These discrepancies can be related to the position of the thermistors on the underside of the chip as explained in chapter 3.

The above Figures further illustrate the temperature difference between the upper and the lower surfaces of the board, data that have not been available in any of the previous work of [31]. This differential temperature is a maximum at the leading edge, and increases with velocity. The IR curves for the top of the board show regular variations which increase with air velocity, whilst the curves for the back of the board are more uniform with only slight variations. This is most likely to be the result of increased turbulence due to complex surface geometry (height of the package on the top surface). Closer analysis of these figures also reveals that the board is an important contributory factor to the development of the thermal wake, and must be included in any thermal analysis. This is discussed in more detail in the next section.

The increased amount of data made available by the thermal image technique made

it possible, to carry out direct comparisons between the results from these experiments and temperature predictions from the FE model of 13 modules in a row presented by [31]. Figures 6.15a-c shows the comparison of the FE model predictions with thermistor and IR respectively. Analysis of these figures indicates that the temperature difference between the top and under surface of the board predicted from the FE model is too high. This is because the complicated multi layer PCB was modelled simply, by weighting the conductivity of the board (considered parameter system) in the x and y directions [31]. Also in the FE model the leads from the active layer of the chip were constructed to stop on the top surface of the board. However in the real PCB these leads penetrate the board and are soldered to copper tracks on its under surface. Before modification of the FE model, the FE model predicted lower temperatures directly below the module on the board (air gap between the package and board). This was found to be the result of assuming convection in this area [31].

6.10.2 MODIFICATION OF THE FE MODEL

In an attempt to improve the FE model and to remove the discrepancies between the experimental values and the original FEM model mentioned above, the FE model was modified as follows:-

a) Since it can be shown that up to 65% of the generated heat can be conducted down to the board, a central layer of 0.05mm copper was constructed in the board under each module. This was based on the hypothesis that, most of the copper tracks within the multi layer board run laterally from individual modules to the connector at the edge of the board. Thus there is no conduction path in the board between neighbouring modules Figure 6.16 a and b. This modification replaced the lumped conductivity values in the original FE model presented by Hardisty et el [31].

b) The leads from the active layer of the package were continued through the

board to the under side of the PCB.

c) Convection from the top surface of the board, directly below the modules, was removed.

Figure 6.17a illustrates the comparison between the temperatures predicted by the improved FE model, and the experimental values from both the IR thermometer and the thermistors on the upper surface of the PCB. Similar comparison are also shown in Figure 6.17b for the under surface of the PCB. Both Figures show the closer fit between the improved FE model and the experiment values for uniform power conditions. However further work was required, as correct FE predictions are particularly important for conditions of non-uniform power.

6.11 CONVECTIVE HEAT TRANSFER - ANALYSIS OF THERMAL WAKE

6.11.1 DEFINITION OF THE HEAT TRANSFER COEFFICIENT

The rate (Q) at which heat is transferred by convection from a solid surface of area A and of temperature T_s, to an adjacent fluid at an ambient temperature T_f was defined in equation 3.9 Chapter 3.

Rate equation serves as a definition of the heat transfer coefficient h which may then be deduced empirically from experimental data:-

$$h = \frac{\dot{Q}}{A(T_s - T_f)} = \frac{\dot{q}}{(T_s - T_f)} \qquad (6.7)$$

Although h cannot be regarded as a true transport property of the fluid, its value depends only on fluid properties and the dynamic state of the fluid local to the

surface. Provided that the thermodynamic properties are independent of temperature, then the great power of the h concept is that, in the steady-state, its value is independent of either the temperature difference (T_s-T_f) or the heat flux q.

6.11.2 THE APPROPRIATE VALUE OF THE LOCAL AMBIENT FLUID TEMPERATURE

At the inception of this research it was thought that the evaluation of h from equation 6.7 would be straightforward. The surface area A of the electronic package was known and both the power dissipation Q and the surface temperature T_s were measured in each experiment. Only the measurement of the ambient temperature was required. Unfortunately, for air flowing over an array of electronic modules, arbitrarily powered, the air temperature rise along the duct is capable of different interpretations.

The steady-flow energy balance equation may be written

$$\sum Q = mC_p(T_b - T_i) \qquad (6.8)$$

This equation may be regarded as a definition of the bulk mean temperature of the fluid, T_b. This mean temperature is difficult to evaluate experimentally (a traverse is required), instead experimental values of m and Q are used in equation 6.8 to calculate the value of T_b (this implies perfect transverse mixing).

$$\overline{T_b} = T_i + \frac{\sum \dot{Q}}{\dot{m}\ C_p)} \qquad (6.9)$$

It should be noted that for this research, the power dissipation levels used were low, and the mass flow rates relatively high, so that the total rise of the bulk fluid temperature through the duct was quite small (1 or 2°C) in comparison with the temperature difference (T_s-T_f).

In fact this research has shown that transverse mixing of the coolant in the channel is poor. Flow visualisation experiments, and CFD simulations, have demonstrated that the fluid field may be sub-divided into three characteristic regions. Heat convected from the surface is confined to a rather thin layer of fluid immediately adjacent to the modules, and is convected downstream in the form of a wake. The mainstream flow is separated from the modules by the wake, and tends to pass through the duct with little interaction, almost as a bypass. The flow which separates from the trailing edge of each module forms zones of recirculation between adjacent modules.

Thus in the evaluation of h from equation 6.7, there are a number of possible choices for the local ambient fluid temperature T_f. In most of the experimental research at Bath, the bulk mean air temperature T_b was calculated from equation 6.9. Some researchers use the free stream temperature outside the boundary layer. This parameter was considered, but the difficulties of carrying out a temperature traverse across the duct without altering the flow itself caused its rejection.

Other investigators use the duct inlet temperature T_i as the reference temperature. Because for the present conditions the air temperature rise through the duct is small, there is little difference between T_i and T_b.

6.11.3 The EFFECT OF THE HEATED WAKE ON THE TEMPERATURE OF DOWNSTREAM MODULES

For the case of fluid dynamically fully developed flow, when the flow conditions are identical for all modules, h should have a constant value which is independent of the position of the module. This proposition was validated by Hardisty et al [31]. For a single powered module, for fully developed flow, h values for modules in different rows were found to be identical.

Next, consider the important datum case of fully developed flow, but with all modules uniformly powered, also investigated by Hardisty et al [31]. Because the temperature of the thermal wake increases progressively in its passage downstream, the surface temperature of the modules was also found to increase. When the bulk temperature of the fluid, (defined by equation 6.9) was used to calculate h, this h value decreased with downstream distance (because the temperature difference (T_s-T_b) increased). Considerations such as these, when upstream wake effects, appear to change downstream h values, prompted a change of methodology.

6.11.4 SUPERPOSITION -SEPARATING OUT THE WAKE EFFECTS

Provided that the properties of the fluid are essentially independent of temperature then the thermal energy equation of the boundary layer is linear and homogeneous, Shah and London [74]. In this case the sum of solutions to the temperature field is again a solution of the energy equation. This principle of superposition may be used to justify the proposal by Moffat [75] to equate the total temperature rise of a module to the sum of two separate effects:-

$$T_s - T_i = (T_{LA} - T_i) + (T_s - T_{LA}) \qquad (6.10)$$

Where:-

T_{LA}	= Local ambient fluid temperature.
T_i	= Duct inlet temperature.
$(T_{LA} - T_i)$	= Rise in local ambient fluid temperature due to the thermal wakes from upstream elements.
$(T_s - T_{LA})$	= Rise in temperature of the module above T arising purely from the effect of its own power dissipation (adiabatic temperature).

The superposition principle can also be used to justify the calculation of the total wake effect $(T_{LA} - T_i)$ as the sum of the wake effect of individual upstream powered modules. The local temperature rise $(T_s - T_{LA})$ must be a function only of the power dissipated in the module, and the value of h. This intrinsic value of h should depend only on the local fluid dynamic state of the flow.

6.11.5 INFLUENCE COEFFICIENT USED TO PREDICT THERMAL WAKE

Wills [30] has used an approach similar to that of Moffat [32] to propose that the temperature (T_n) of any module in row n can be expressed by an equation of the form:-

$$T_n = T_A + R_{on}P_n + \sum {}_nZ_i\, P_i \qquad (6.11)$$

Where:-

T_A = Local ambient temperature.
P_n = Power dissipation of row n.
R_{on} = Convective thermal resistance of row n, all other powers zero.
${}_iZ_n$ = Temperature rise at n due to 1 watt power applied at row i.
P_i = Power dissipation at row i, upstream of row n.

${}_iZ_n$ is termed an influence coefficient and is the effect on the ambient temperature at row n of the heated wake from an upstream powered module in row i. The value of the influence coefficient depends only on the relative positions of the rows i and n. Naturally the further downstream n is from i the smaller will be the numerical value of ${}_iZ_n$. Although the temperature of the thermal wake is a function of power, the influence coefficients themselves are independent of power. If a number of modules are powered they each contribute in proportion to their power towards the temperature level of module n. The convective thermal resistance R_{on} is of course equal to (1/hA).

For the particular case when all modules are uniformly powered:

$$T_n = T_A + P_n\,(R_{on} + \sum {}_iZ_n) \qquad (6.12)$$

For the case of fully developed flow, when the value of R_{on} will be the same for all rows, based on equation 6.12, a convenient methods of calculating values of the influence coefficients can be developed. Starting from experimentally measured values of T_n, R_{on} may be calculated directly by noting that for row 1 the influence coefficients are zero (no wakes). Recalling that the value of an influence coefficient depends only on its relative position, then

$_1Z_2 = {}_2Z_3$ ..... $_nZ_{n+1}$ etc. Also see Table 6.2.

In this way the experimental influence coefficients were derived from the leading edge (row 1) to the trailing edge (row 13) of the board see Table 6.3 and Figure 6.18a.

The bulk air temperature at any row can be calculated as described in chapter 3 (energy balance equation) see Table 6.4. The effect of uniform powering means that the bulk air temperature rise with respect to row number is constant thus the bulk air temperature rise at any row, i can be expressed in the form:-

$$\text{BULK AIR TEMP. RISE AT ANY ROW} = \frac{\text{Max. BULK AIR TEMP RISE (i -1)}}{13}$$

6.12 CONSIDERATION OF THE DIP'S SURFACE AS THE THERMAL WAKE SOURCE

In order to verify the effect of the board as a contributing factor to thermal wake, the values of the temperature difference between the local air and DIP surface was predicted using the heat transfer coefficient correlation presented by [31]. The values

for local air temperature produced using this method were higher than the experimental observations; this is probably because the correlation presented by [31] was based on T_{bulk} as the reference fluid temperature for correlation of experimental data. To produce values in agreement with the experimental observations, it was necessary to reduce the value of the Q/A to 983 W/m^2. Using the convective area of the DIP as 0.000126 m^2, this suggested a convected power dissipation of 0.124 W from the top surface of each DIP. For the thermal wakes from the DIPs to account for the observed local air temperature rises the power convected from the top surface of the DIP's upper surface, 0.124 W would only be 10.33% of the total power input to each DIP removed by convection. Clearly this is not possible because of the temperature levels shown on the thermal images. Therefore the thermal wake from each module must be emitted from a much larger area, than just the top surface of the DIP. The printed circuit board must also be contributing significantly. As it can be seen from the thermal images illustrated in Figures 6.13a-c, the top surface of the DIP's is 2 to 3°C higher than the corresponding board temperature nearby. Thus the thermal wake must be emitted from an effective area of the PCB, (board + package) to downstream rows. In essence, the thermal wake cannot be considered to have a small local source, rather, for the present investigation, the effective convective area dissipating the heat from the top surface of the PCB for each DIP must be considered as follows:-

Effective conductive area = [board top surface]+[DIP's side surfaces]

Effective area = [0.035 x 0.015] + 2[(0.021 x 0.003) + (0.006 x 0.003)]

Using the value of the effective area, 0.000678m^2 and the experimentally derived

value of Q/A yields a convective power dissipation of 0.67W, this is equivalent to 56% of the total power input to each DIP which is convected away from the effective area Table 6.5, illustrates values for 2.5 m/s and uniform powering of 1.2 W/chip. These values are of the corrected magnitude and improve agreement with the experimental results.

In a series of FE runs, the effect of the modelled copper layer under each package was investigated. The heat transfer coefficient used in these runs was obtained from the correlation [31] and programmed into the FE model. IR and FE temperature rise with h value based on T_{bulk} is illustrated in Figure 6.18b.

Initially, experimentally determined temperature rises using principal of thermal wake was found to vary erratically between the 6th-8th and 12th-13th row. This erratic variation at the trailing edge of the board was found to be the result of the turbulent edge effect, as it can be seen from Figure 6.14a, the temperature of the 13th row suddenly reduces. Closer analysis of Figure 6.14a also reveals that the discrepancies between the 6th and 8th row are due to cooler operation of these packages. To investigate this, the PCB was removed from the test rig and tested in natural convection, it was found that these packages were faulty, they were replaced for the subsequent tests.

The experimentally derived values of the local air temperature rise were used to model the local air temperature rise in the FE model. This method of analysis was thought to facilitate the investigation of non-uniform powering.

The section of the FE program generating the convection surfaces in the FE model was written in the form of a separate data user file (conv.ufl) as described in chapter 2. This file includes the varying influence coefficients, constant h value for all the rows and the powering coefficients for non-uniform powering. Figure 6.19a illustrates the comparison of IR measured temperature distribution, with the corresponding temperature predictions from the modified FE model for uniform powering at constant h and varying influence coefficients. Similar comparison are also shown in Figure 6.19b for the thermistor measured temperatures. The analysis of these Figures indicates that good agreement exists between the modified FE model and the experiment.

6.13 NON-UNIFORM POWERING

Having successfully verified the FE model for uniform powering, the investigation was extended to non-uniform powering. This involved powering one row of DIPs (row 5) on the PCB. The scan program was initiated to scan the top and under surface of the complete board, thermal image's was produced using the image program as shown in Figure 6.20a and 6.20b respectively. Comparison of the IR and thermistor measured temperatures are shown in Figure 6.21a and 6.21b. Similarly the row 5 of the FE model was powered, Figure 6.22a and 6.22b illustrate comparison of the surface temperature distribution produced by IR with the corresponding temperatures predicted by the FE model. The results show that an acceptable agreement exists between the modified FE model predictions and that of the experiment for non-uniform powering conditions.

6.14 CONCLUSIONS

1) A mechanical scanner was designed and developed to drive the sensing head of an IR thermometer and to collect data for the temperature array file. This was an alternative to expensive commercially available thermal imaging systems. The scanner was also tested for positional accuracy and backlash.

2) The electronic control system functioned well and software was also developed to control and drive the scanner.

3) The software was developed to generate a thermal image from the temperature array file. This provided adequate capability to allow complete analysis of a thermal image.

4) The research rig was modified to incorporate the scanner. Plastic film fitted to the upper surface of the test duct provided a cheap and effective IR window.

5) Because of the amount of data available on each thermal image, the IR thermal image provided an effective means of verifying the FE model and providing detailed temperature maps of the packages and board. Such detailed data are quite scarce.

6) Modifications to the FE model were successfully to investigate the theory of thermal wake and to alleviate the inconsistencies between FE predicted temperature distribution and experimentally measured values.

7) The IR scanner showed the differential temperature between the top and under surface of the board, in the region nearest the leading edge this temperature difference is a maximum this was thought to be the result of increased turbulence because of the package height. As expected this was not predicted by the FE model, a fluid modelling technique is required to investigate this phenomenon.

8) Good agreement was obtained between temperature predictions from the FE model and the experiment results, for both uniform and non-uniform conditions. This increased confidence in the theoretical treatment of the thermal wake.

ROW no	DISTANCE mm *	h = W/m^2 K $h_x = V^{0.8}/X^{0.4}$	TLOC ** °C
1	7.5	108.1	0
2	22.5	69.7	$({}_1Z_2) = ({}_1Z_2)$
3	37.5	56.8	$({}_1Z_3)+({}_2Z_3) = ({}_1Z_2+{}_1Z_3)$
4	52.5	49.6	" $= ({}_1Z_2+{}_1Z_3+{}_1Z_4)$
5	67.5	44.9	" $= ({}_1Z_2+{}_1Z_3+{}_1Z_4+{}_1Z_5)$
6	82.5	41.4	"
7	97.5	38.7	"
8	112.5	36.5	"
9	127.5	34.8	"
10	142.5	33.3	"
11	157.5	32.0	"
12	172.5	30.8	"
13	187.5	29.8	"

* T_{LOC} =Local air temperature rise due to the sum of thermal wake of powered row
** DISTANCE = Distance from leading edged area mm.

TABLE 6.2- EVALUATION OF INFLUENCE COEFFICIENTS

ROW no.	Constant h value W/m^2 K	DIP temp.rise (Exp)	row 1's thermal wake	T_{LOC} * ΣTHERMAL WAKE
1	108.1	20.0	0.0	0.0
2	"	25.0	5.0	5.0
3	"	28.2	3.2	8.2
4	"	30.8	2.6	10.8
5	"	32.8	2.0	12.8
6	"	34.5	1.7	14.5
7	"	35.8	1.3	15.8
8	"	37.0	1.2	17.0
9	"	38.1	1.1	18.1
10	"	39.0	0.9	19.0
11	"	39.8	0.8	19.8
12	"	40.6	0.8	20.6
13	108.1	39.8	0.0	0.0

KEY: * T_{LOC} = LOCAL AIR TEMPERATURE RISE

TABLE 6.3- EXPERIMENTALLY DERIVED LOCAL AIR TEMP. RISES DUE TO THE THERMAL WAKE, POWER 1.2W/CHIP (V = 2.5 M/S)

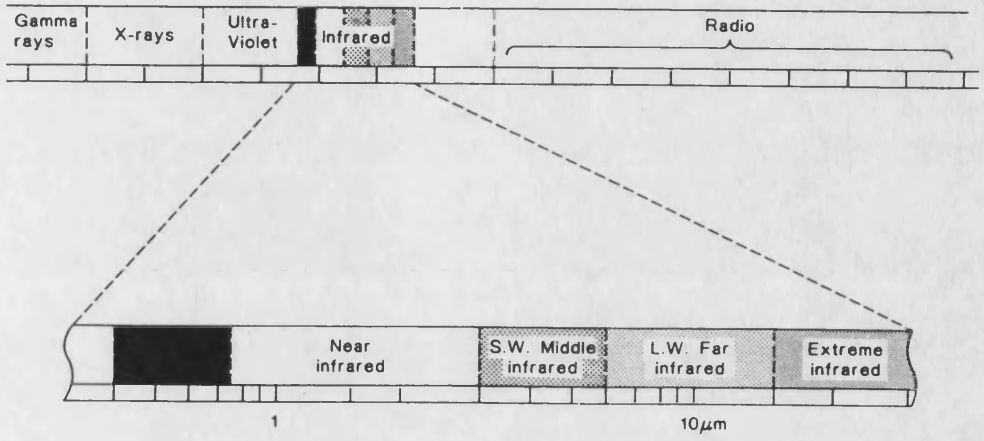
AIR VELOCITY m/s	BULK AIR TEMPERATURE RISE °C
2.5	6.0
3.8	3.5
5.0	2.8

TABLE 6.4 - BULK TEMPERATURE CALCULATION

ROW no.	h value W/m^2 K	DIP TEMP.RISE θ Q/A = 983	row 1's thermal wake	T_{LOC} * ΣTHERMAL WAKE
1	108.1	19.0	0.0	0.0
2	69.7	24.0	5.0	5.0
3	56.8	27.2	3.2	8.2
4	49.6	29.7	2.5	10.7
5	44.9	31.8	2.1	12.8
6	41.4	33.7	1.9	14.7
7	38.8	35.3	1.6	16.3
8	36.6	36.8	1.5	17.8
9	34.8	38.2	1.4	19.2
10	33.3	39.5	1.3	20.5
11	32.0	40.6	1.1	21.6
12	30.8	41.7	1.1	22.7
13	29.8	42.8	1.1	23.8
KEY: * T_{LOC} = LOCAL AIR TEMPERATURE RISE				

TABLE 6.5 - THE LOCAL AIR TEMPERATURE RISES DUE TO THE THERMAL WAKE, USING THE CORRELATION [31] AND EXPERIMENTALLY DERIVED VALUE OF Q/A POWER 1.2W/CHIP (V= 2.5 M/S)

FIGURE 6.1 - ELECTRO-MAGNETIC SPECTRUM



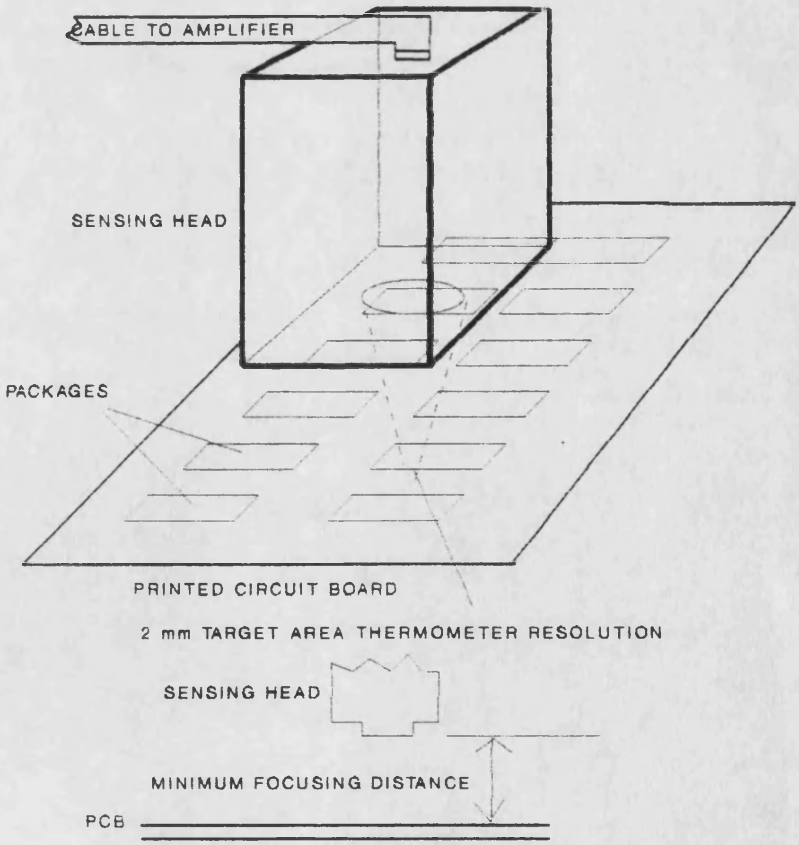


FIGURE 6.2 - DESIGN PROBLEM

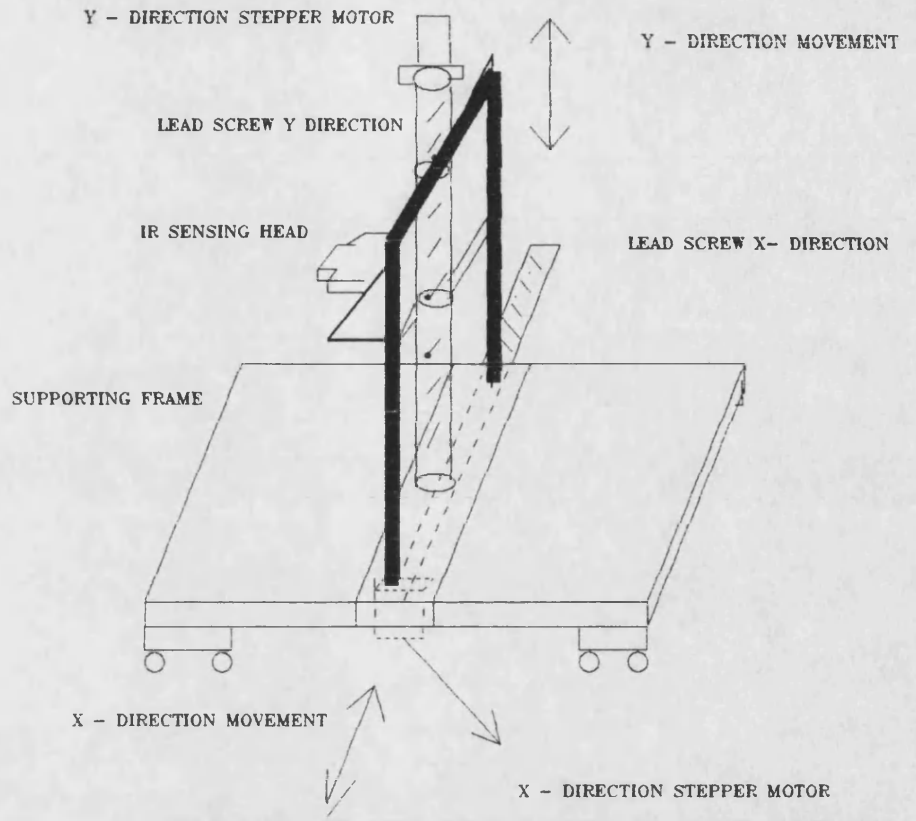


FIGURE 6.3 – TRAVERSE GEAR EARLY SCANNER DESIGN

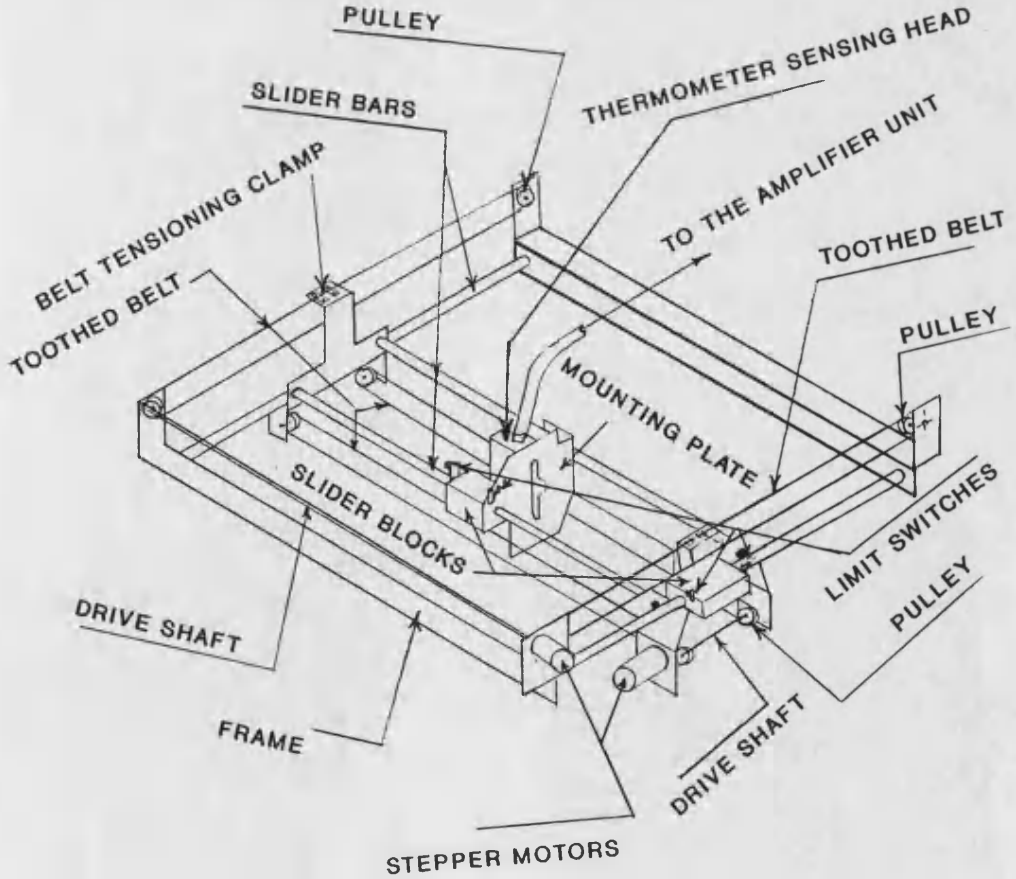
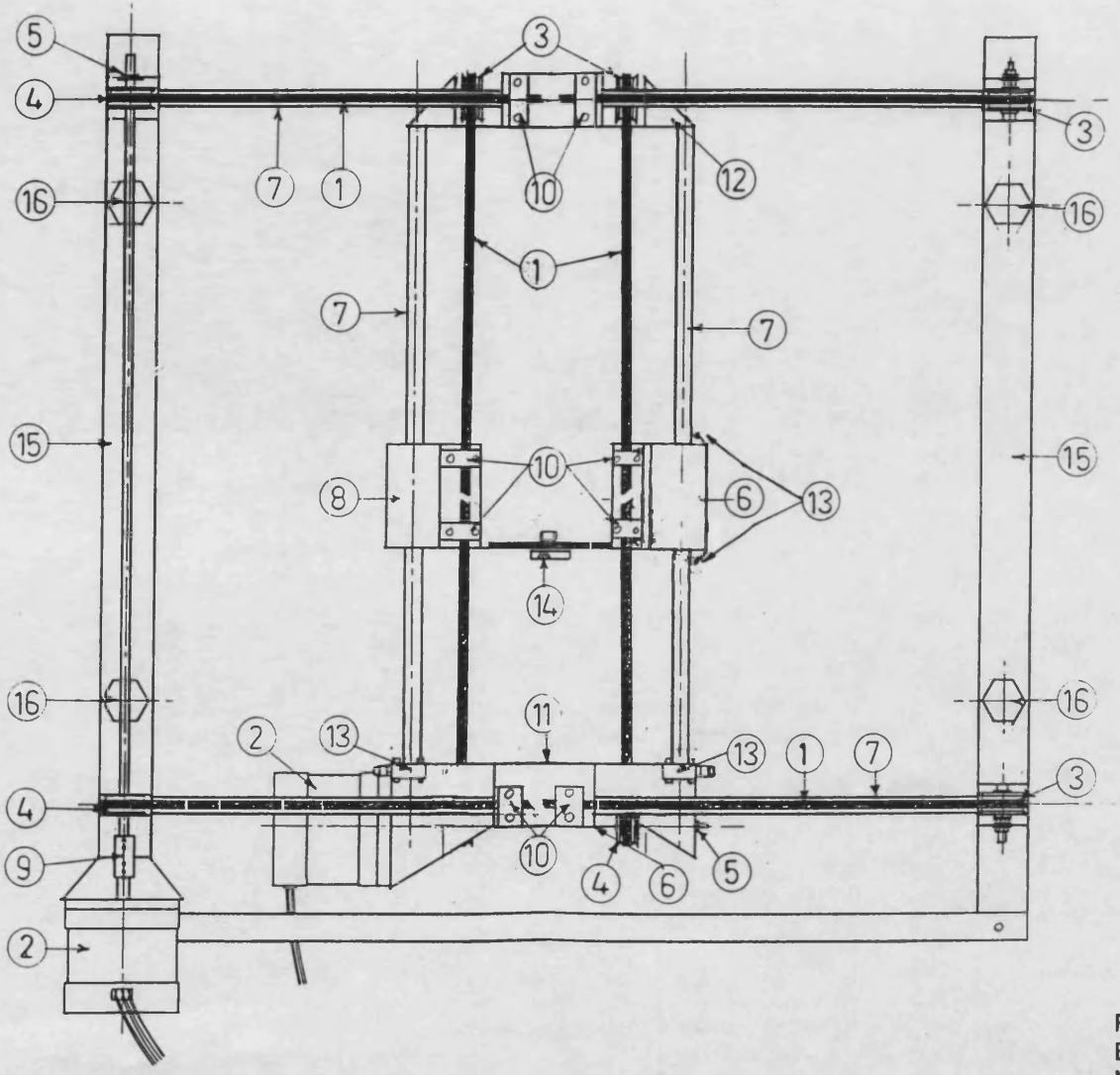


FIGURE 6.4 - SCANNER TOOTHED BELT DESIGN



NO.	DESCRIPTION
1	TOOTHED BELT
2	STEPPER MOTOR
3	IDLER PULLEY
4	DRIVE PULLEY
5	OILITE BUSH
6	SLIDER BLOCK
7	SLIDER BAR
8	SLIDER BLOCK
9	SHAFT CLAMP
10	BELT CLAMP
11	ROLLER END PLATE
12	SLIDER END PLATE
13	LIMIT SWITCH
14	THERM. MOUNTING PLATE
15	ALUMINIUM ANGLE
16	LEG BOLTS

SCALE 1:2

FIGURE 6.5 - ENGINEERING DRAWING MECHANICAL SCANNER

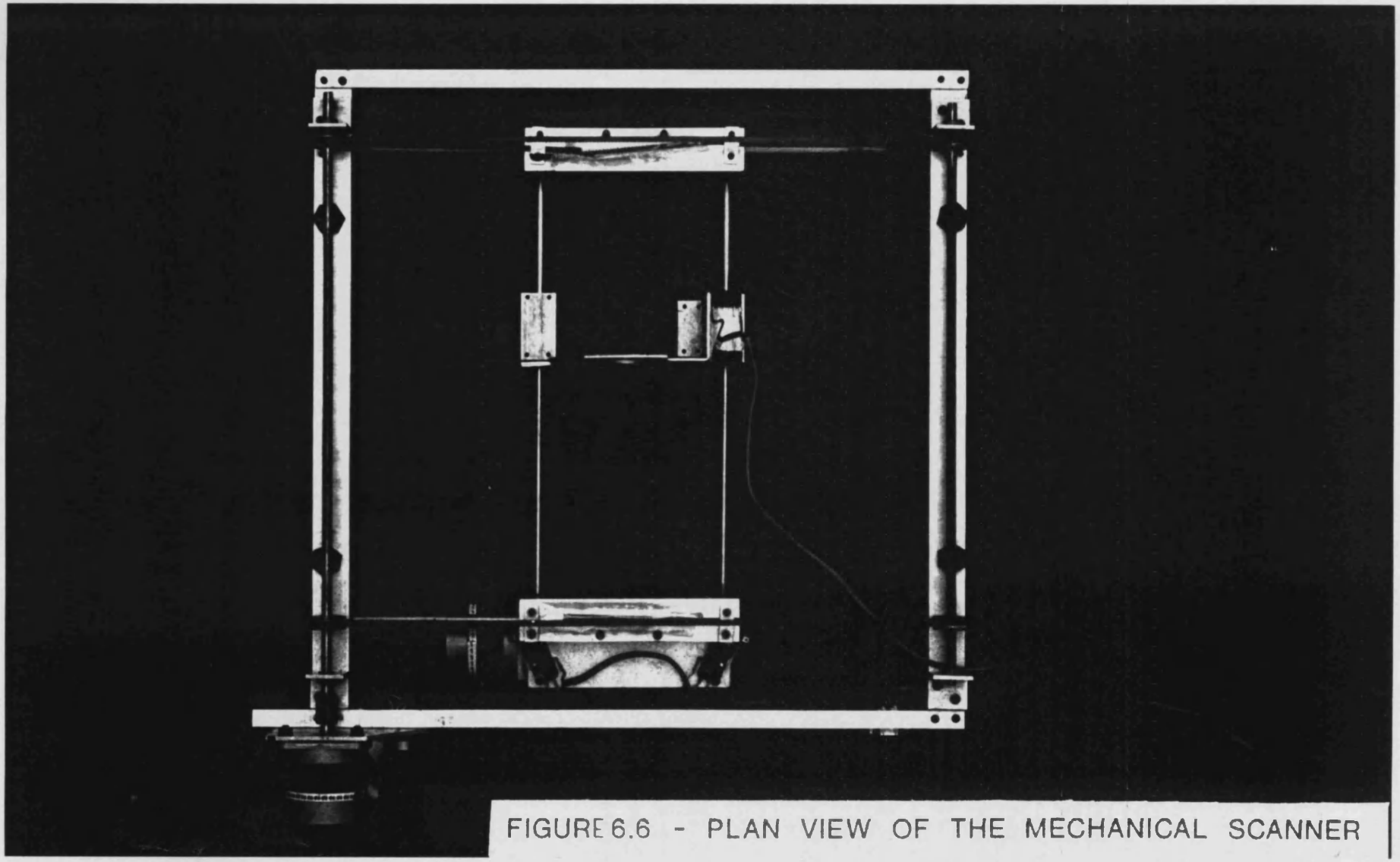


FIGURE 6.6 - PLAN VIEW OF THE MECHANICAL SCANNER

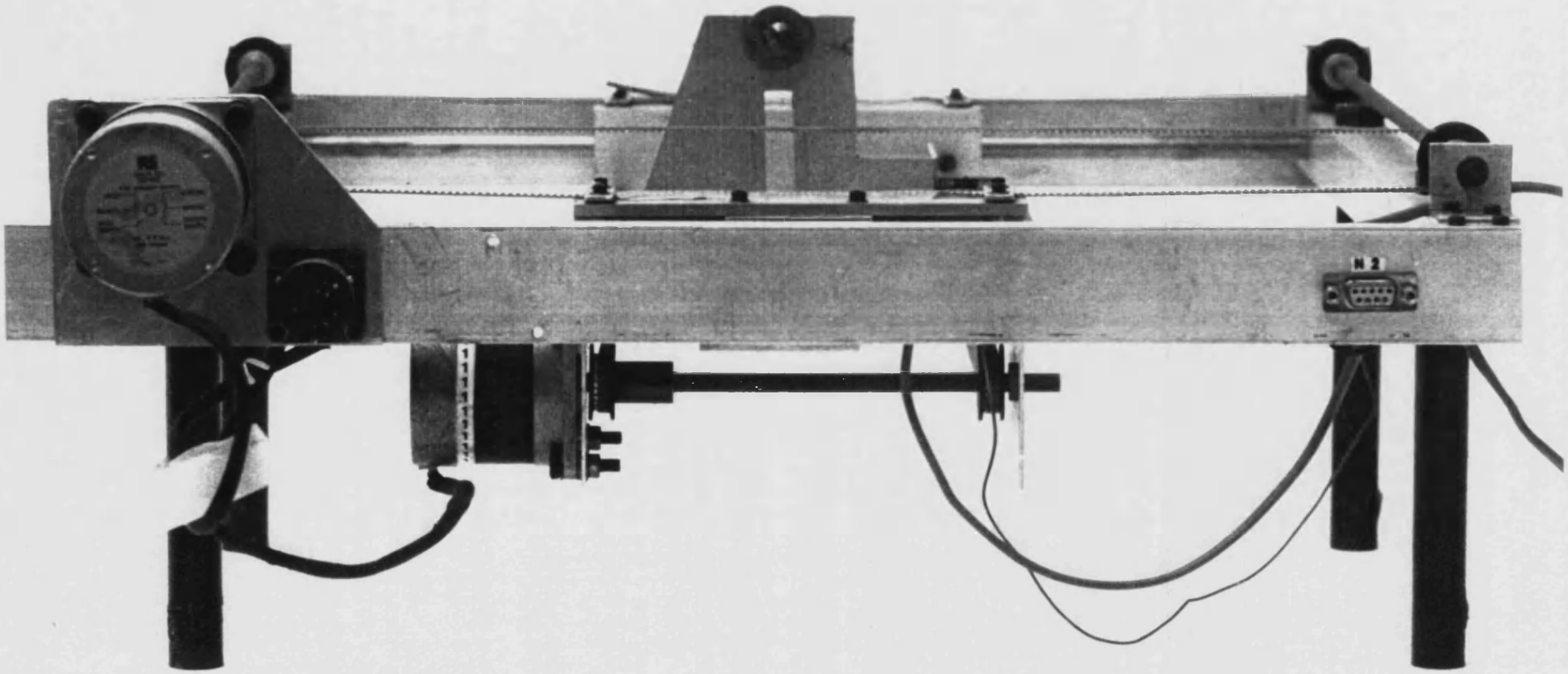


FIGURE 6.7 - DRIVE SYSTEM

FIGURE 6.8 - SCANNER CONTROL SYSTEM

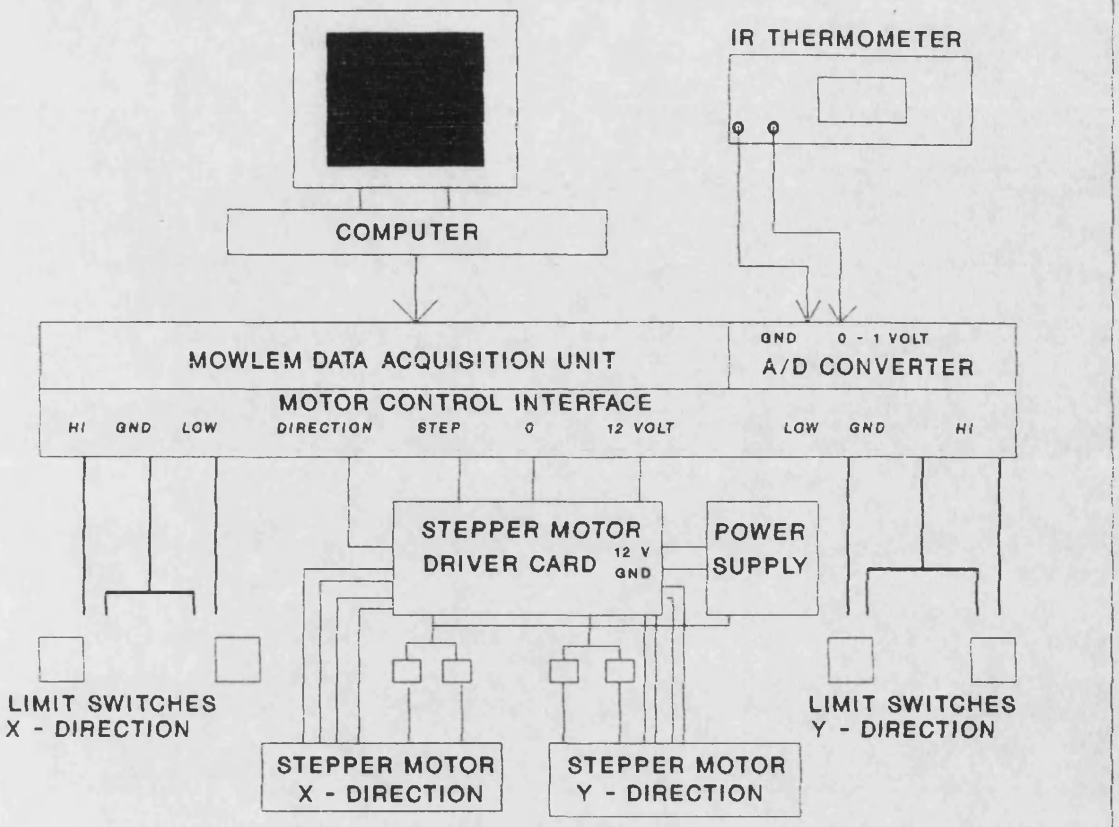
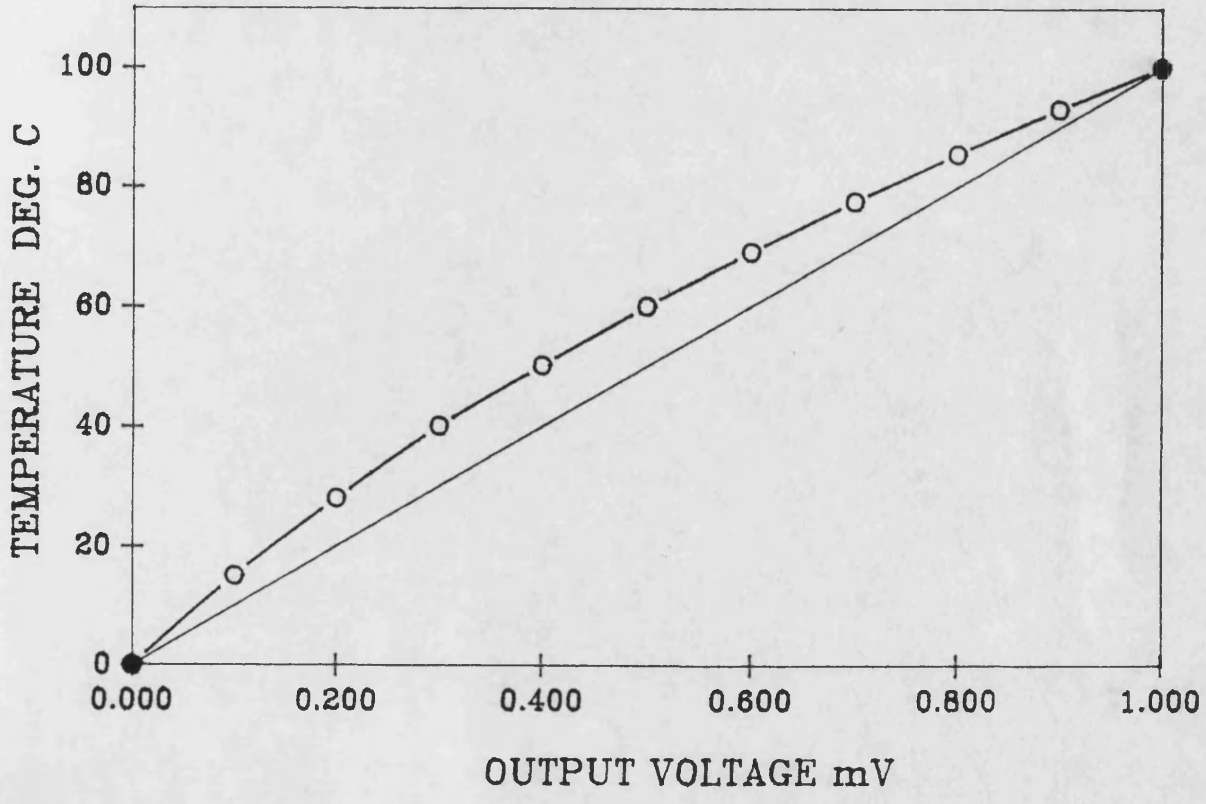


FIGURE 6.9 – THE NON–LINEAR CHARACTERISTICS OF THE IR THERMOMETER OUTPUT WITH TEMPERATURE



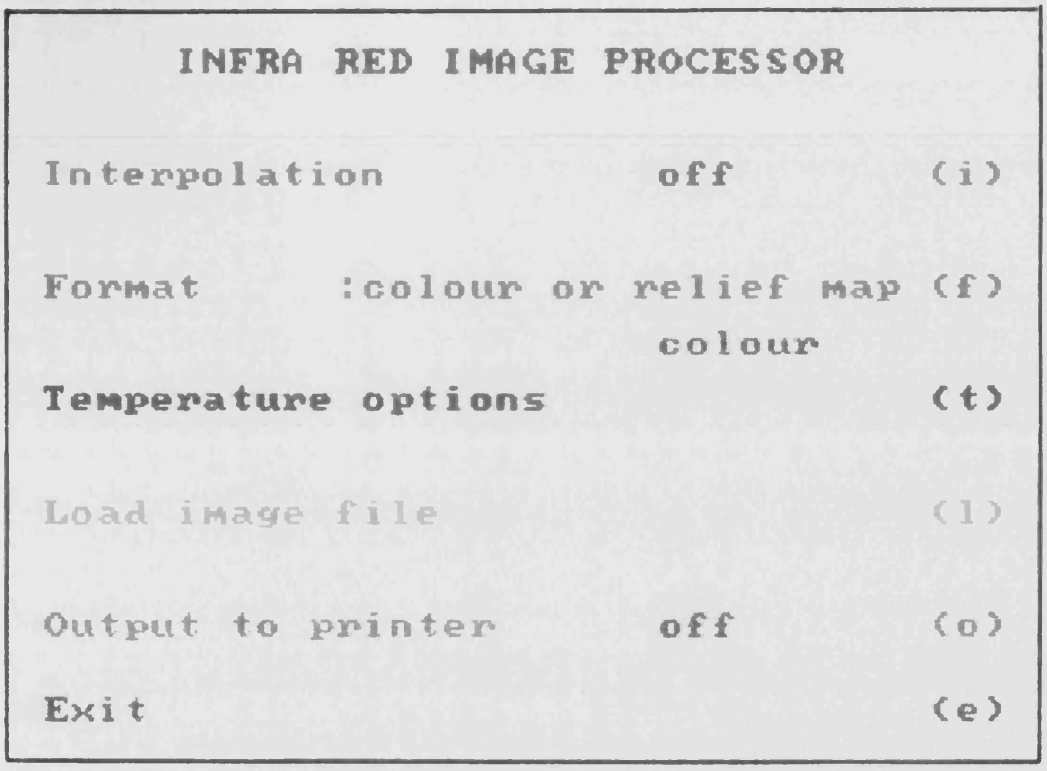


FIGURE 6.10a - FIRST LEVEL MENU
(MAIN MENU)

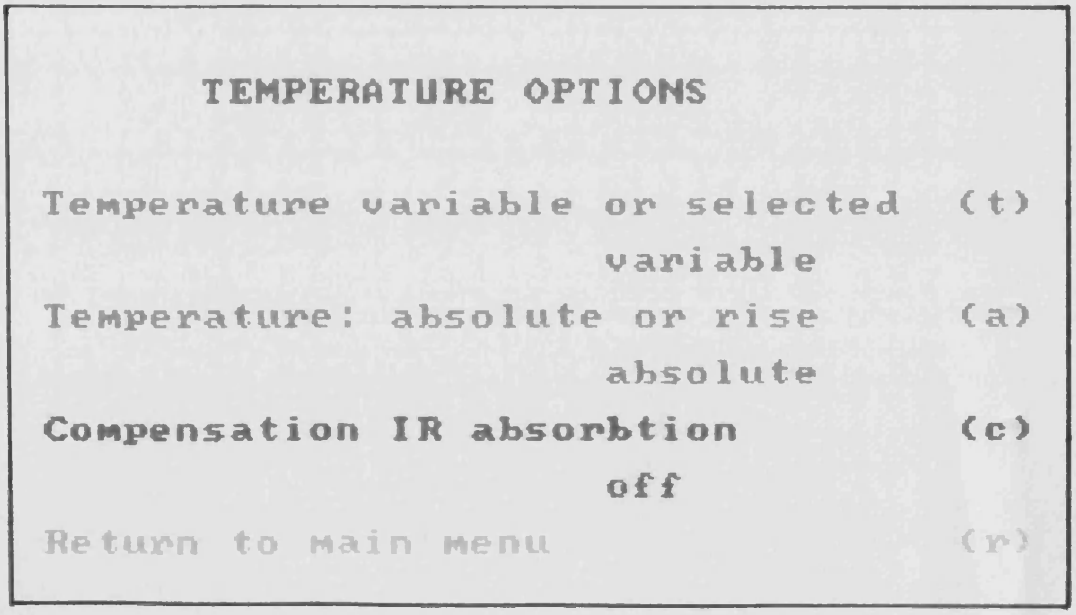


FIGURE 6.10b - SECOND LEVEL MENU -
(TEMPERATURE OPTION)

```
`INFRA RED IMAGE PROCESSOR

Interpolation                          (i)

Format      :colour or relief map      (f)

Temperature options                    (t)

Plot image                             (p)

Output to printer                      (o)

Exit                                   (e)
```

FIGURE 6.10c - THIRD LEVEL MENU -
AFTER THE TEMPERATURE ARRAY
FILE HAS BEEN LOADED

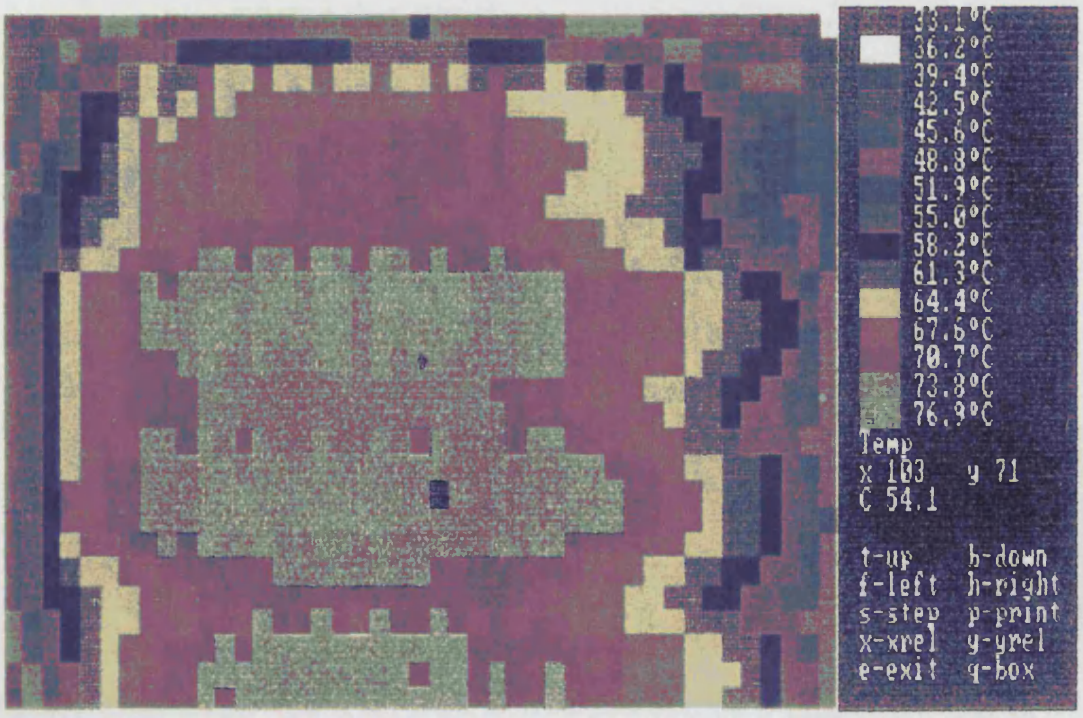


FIGURE 6.10d - THERMAL IMAGE OF EURO-CARD
IN NATURAL CONVECTION
(INTERPOLATION OFF)(POWER 0.6 W/CHIP)

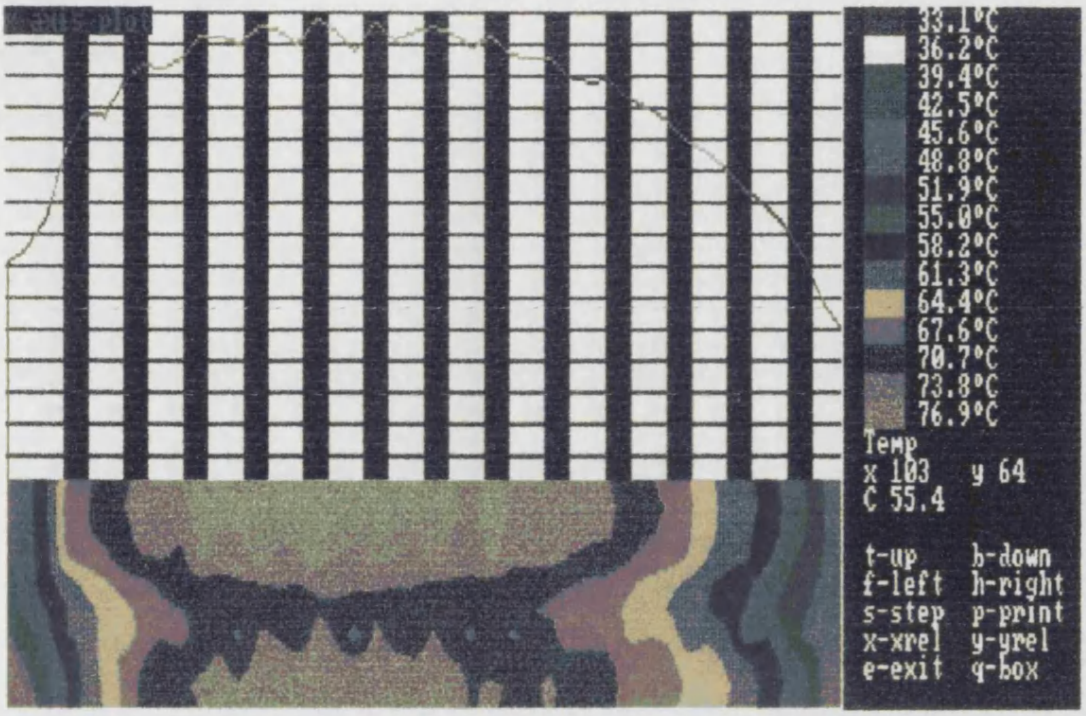


FIGURE 6.10e - TEMPERATURE RISE IN X-DIRECTION WITH REFERENCE TO CURSOR POSITION

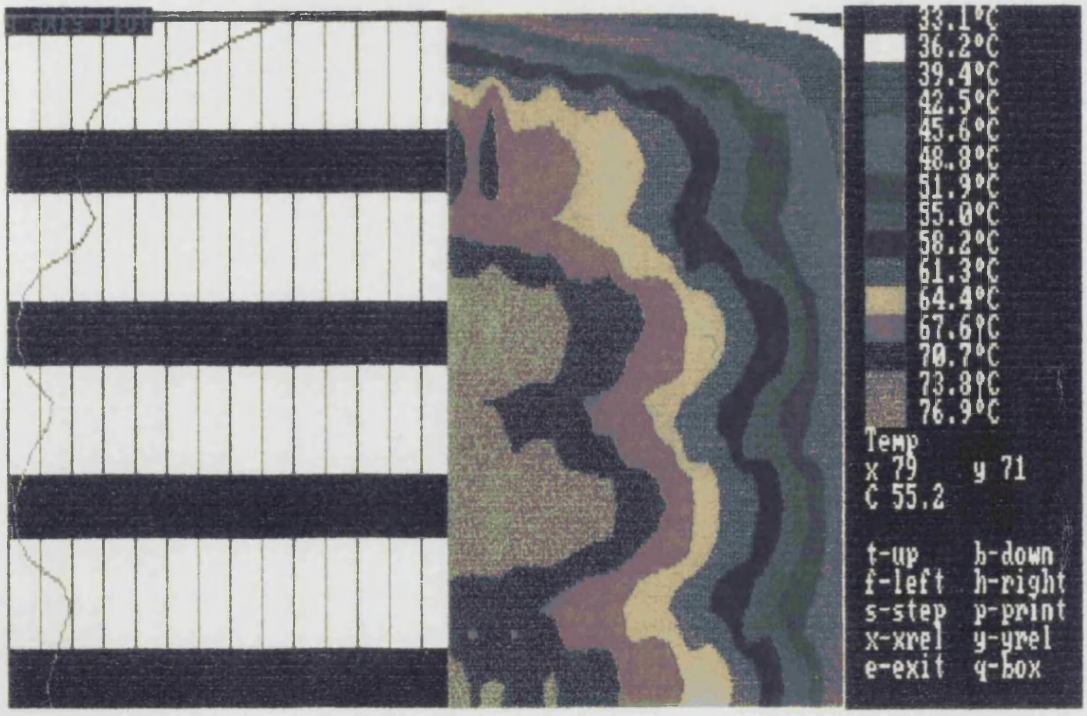


FIGURE 6.10f - TEMPERATURE RISE IN Y-DIRECTION WITH REFERENCE TO CURSOR POSITION

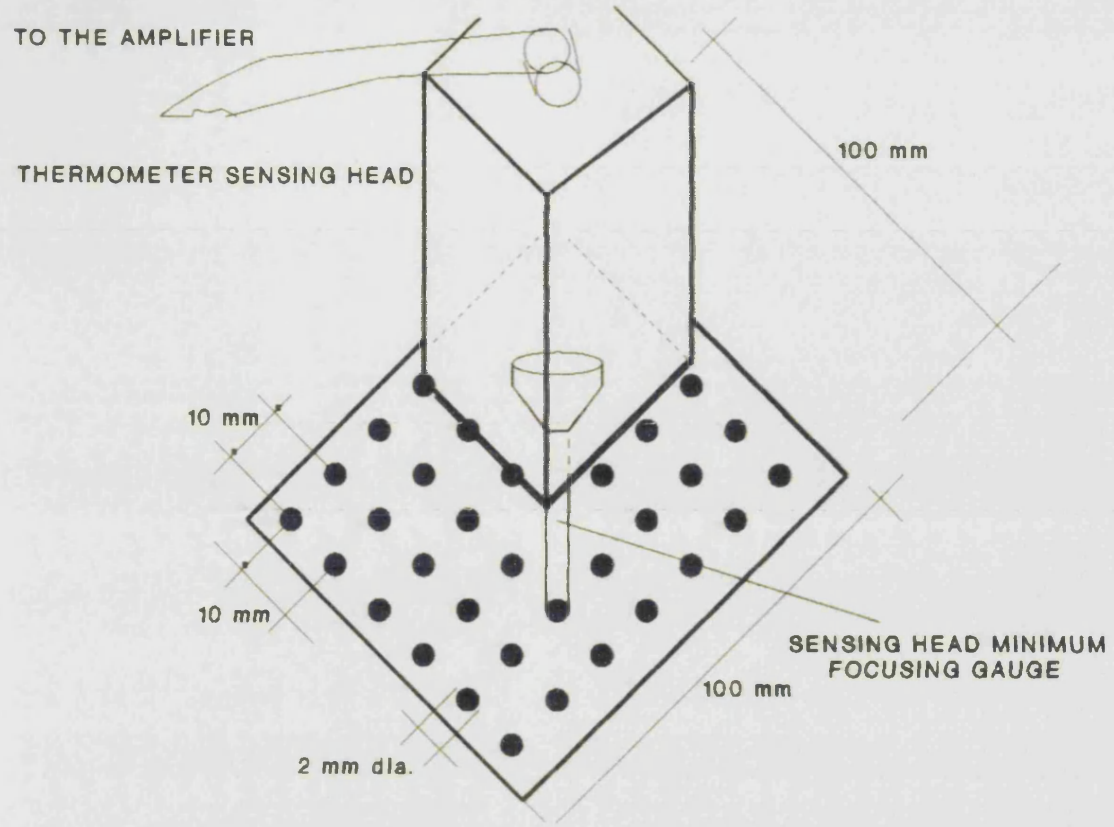


FIGURE 6.11a - POSITIONAL ACCURACY TEST

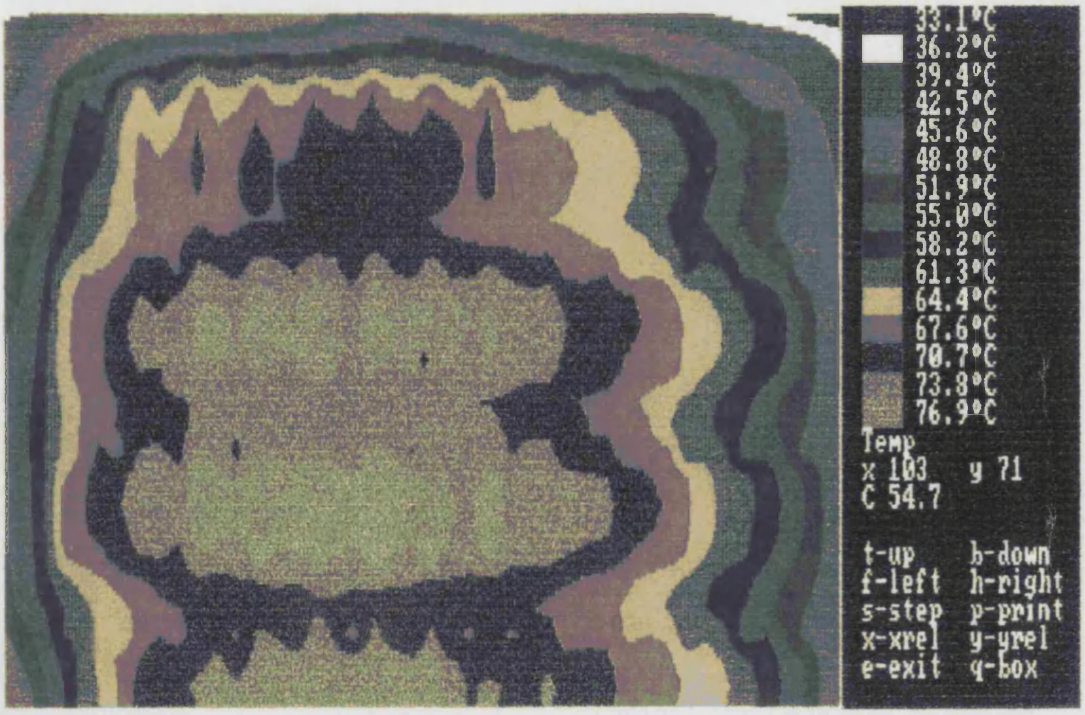


FIGURE 6.11b - THERMAL IMAGE OF EURO-CARD IN NATURAL CONVECTION (POWER 0.6 W/CHIP)

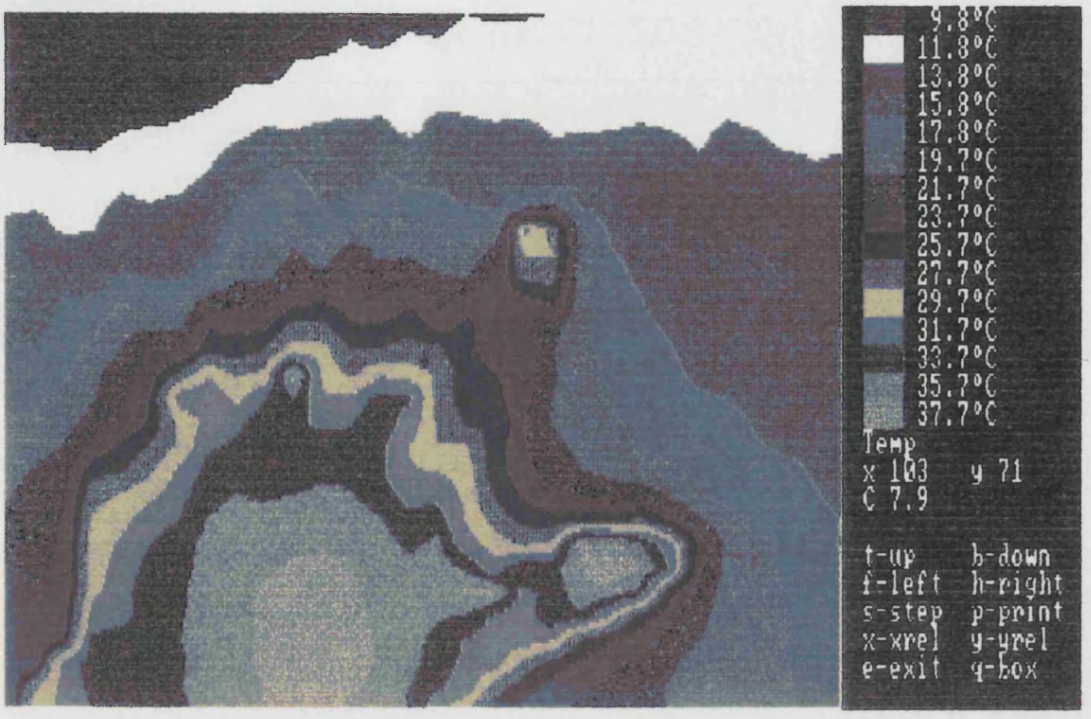


FIGURE 6.11c - THERMAL IMAGE OF A HUMAN HAND (THREE FINGERS TO THE LEFT FOLDED)

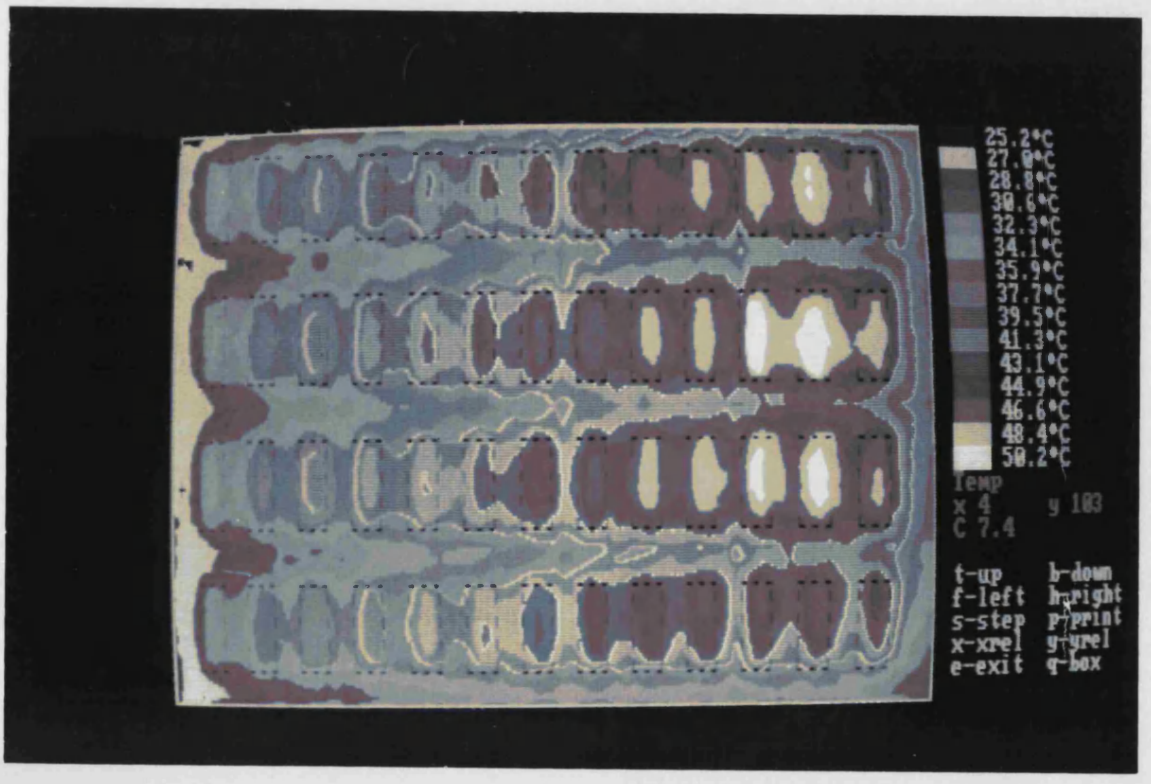


FIGURE 6.11d - CHIP OVERLAY

FIGURE 6.12a -INCORPORATION OF SCANNER TO THE TEST RIG

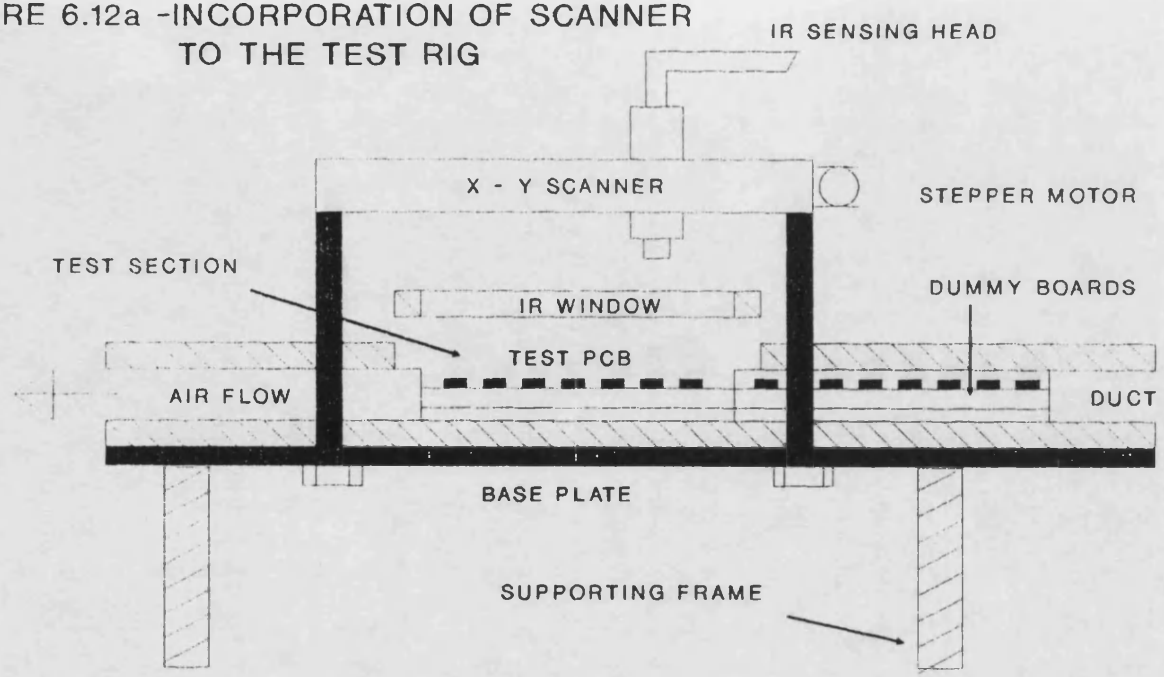


FIGURE 6.12b - IR WINDOW

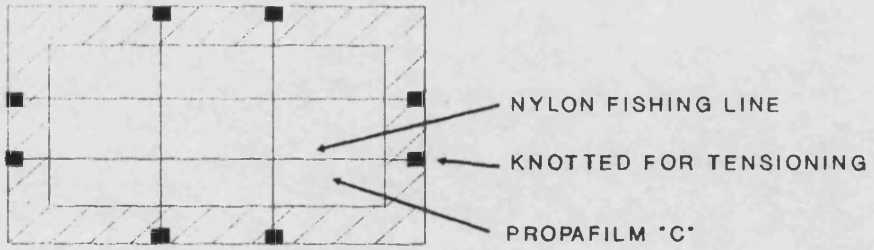
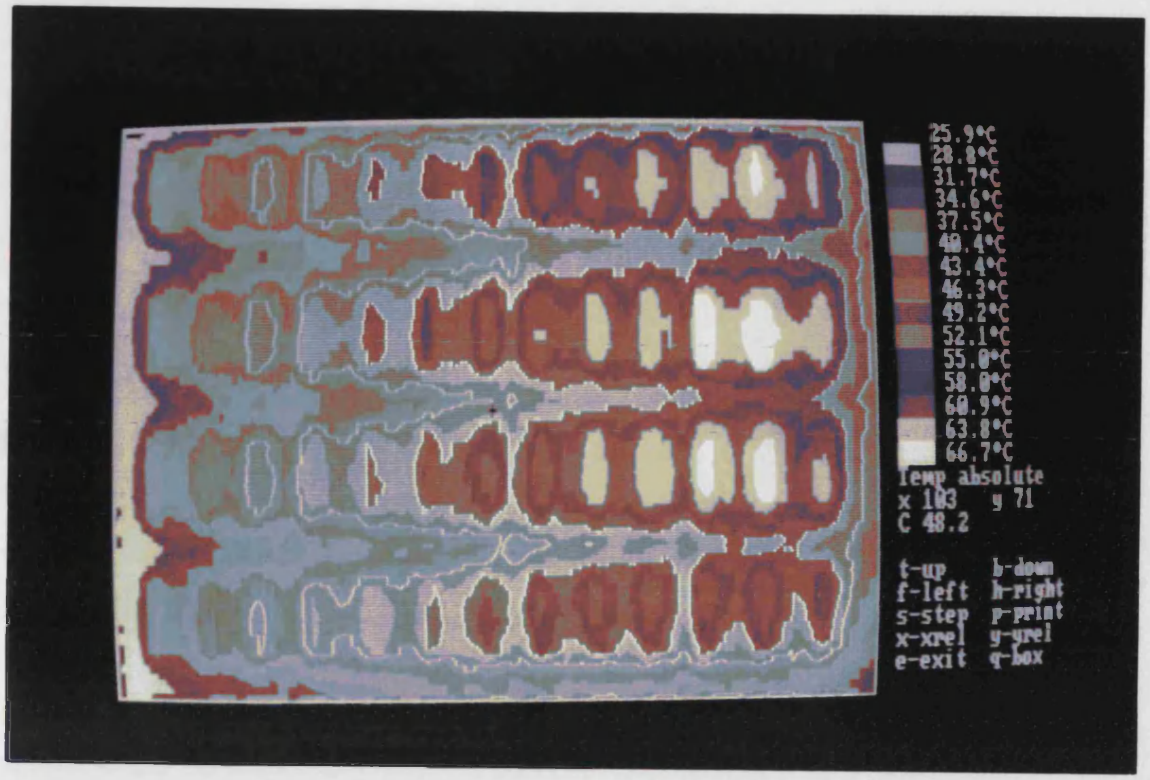
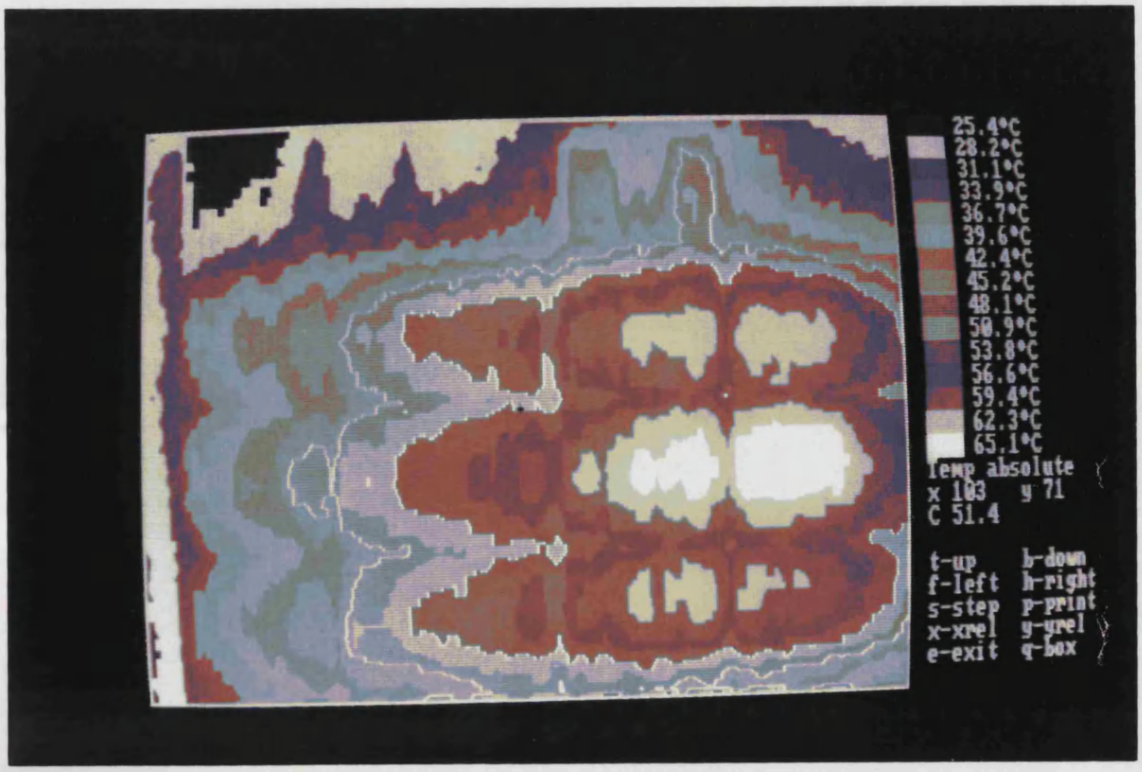


FIGURE 6.13a - THERMAL IMAGE OF THE EURO-CARD
(POWER = 1.2 W/CHIP, V = 2.5 m/s)

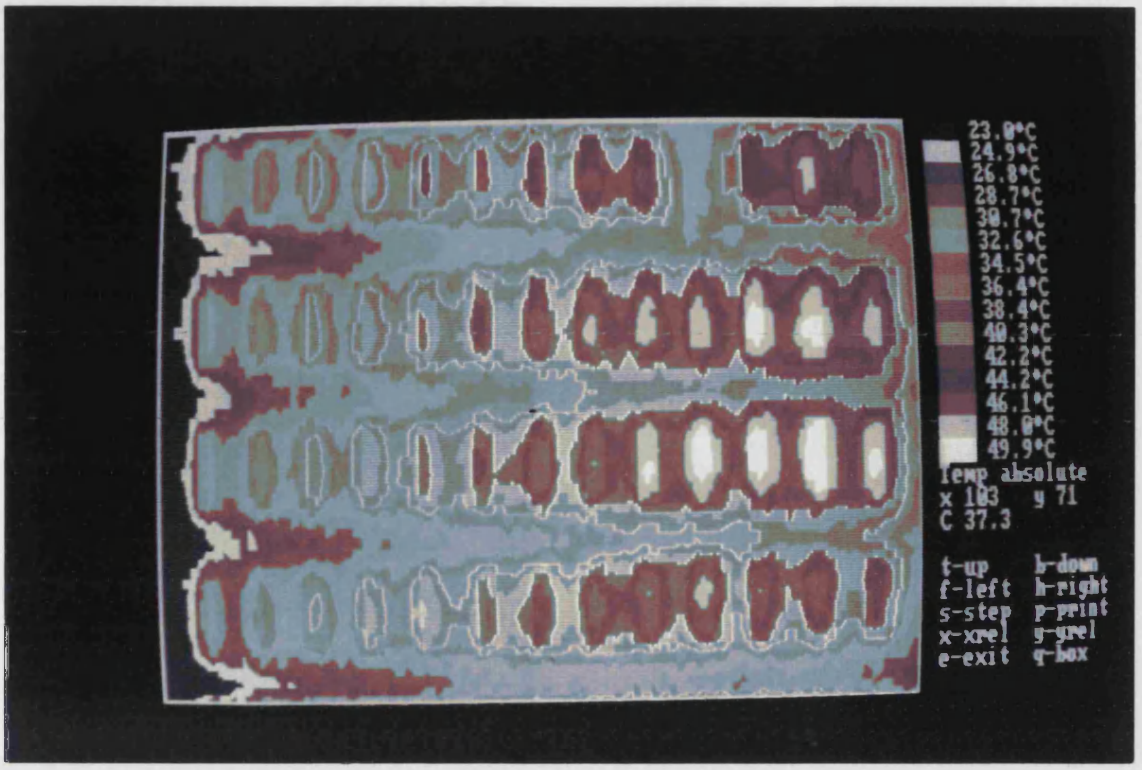


TOP OF THE BOARD

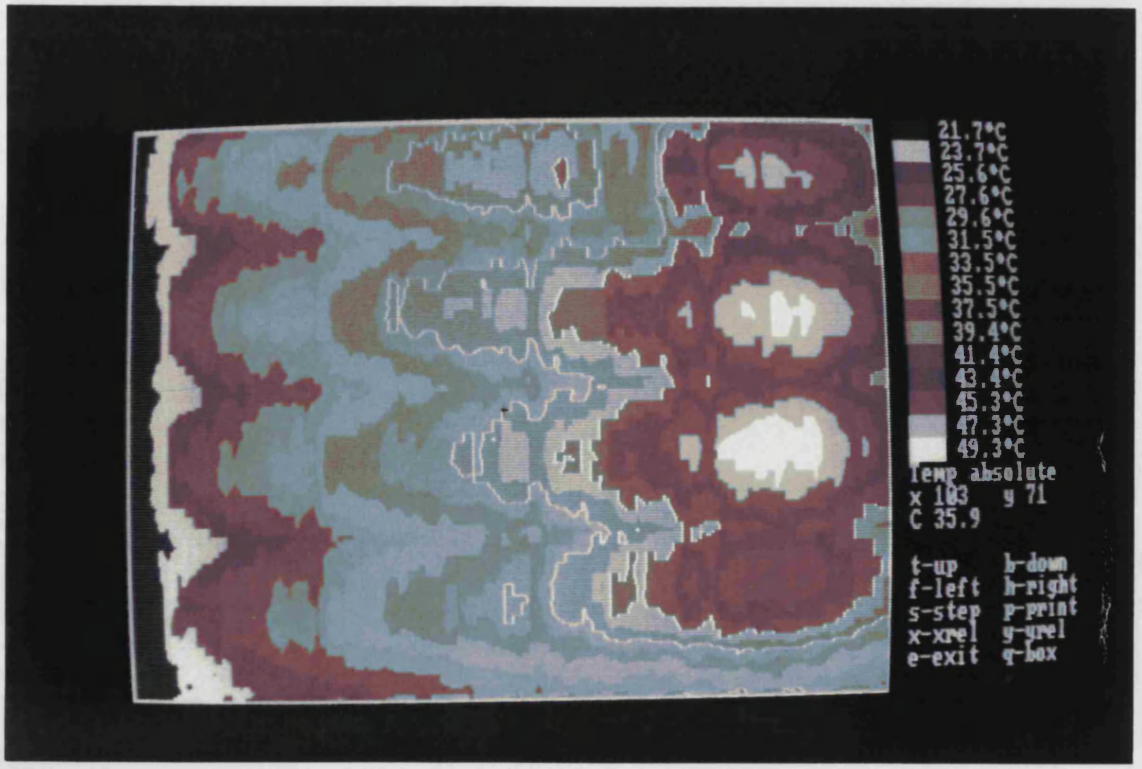


BACK OF THE BOARD

FIGURE 6.13b - THERMAL IMAGE OF THE EURO-CARD
(POWER = 1.2 W/CHIP, V = 3.8 m/s)

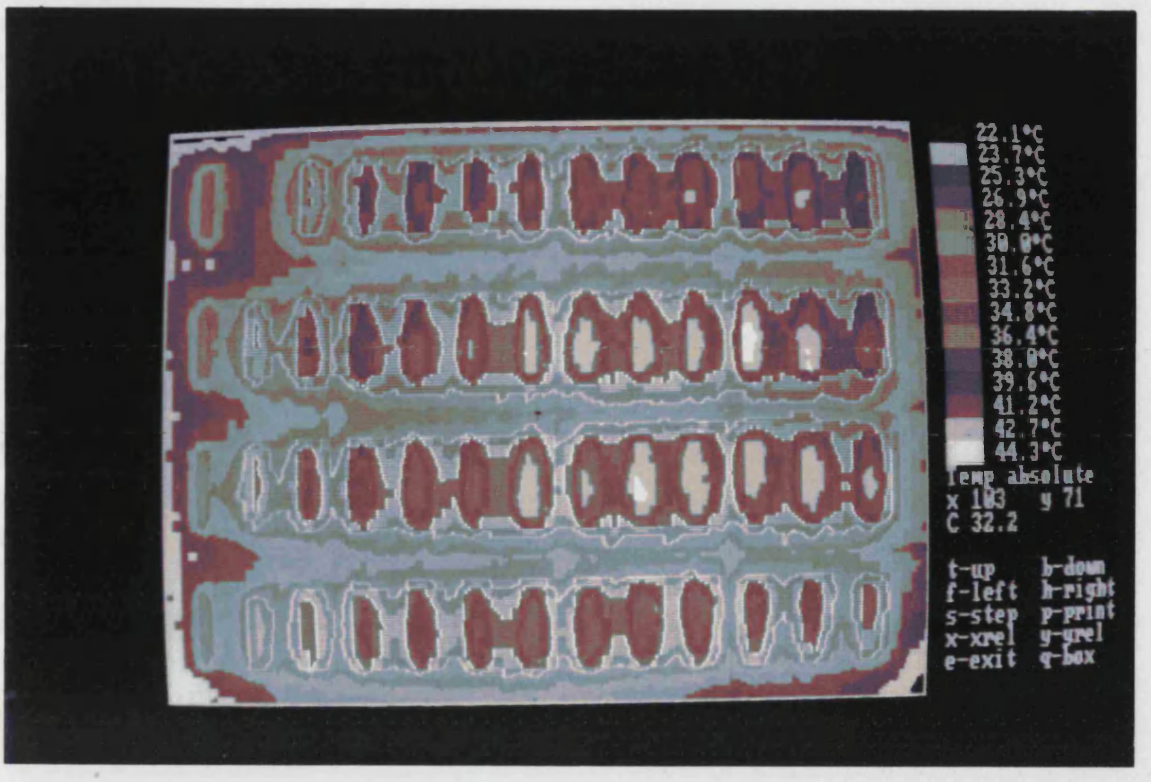


TOP OF THE BOARD

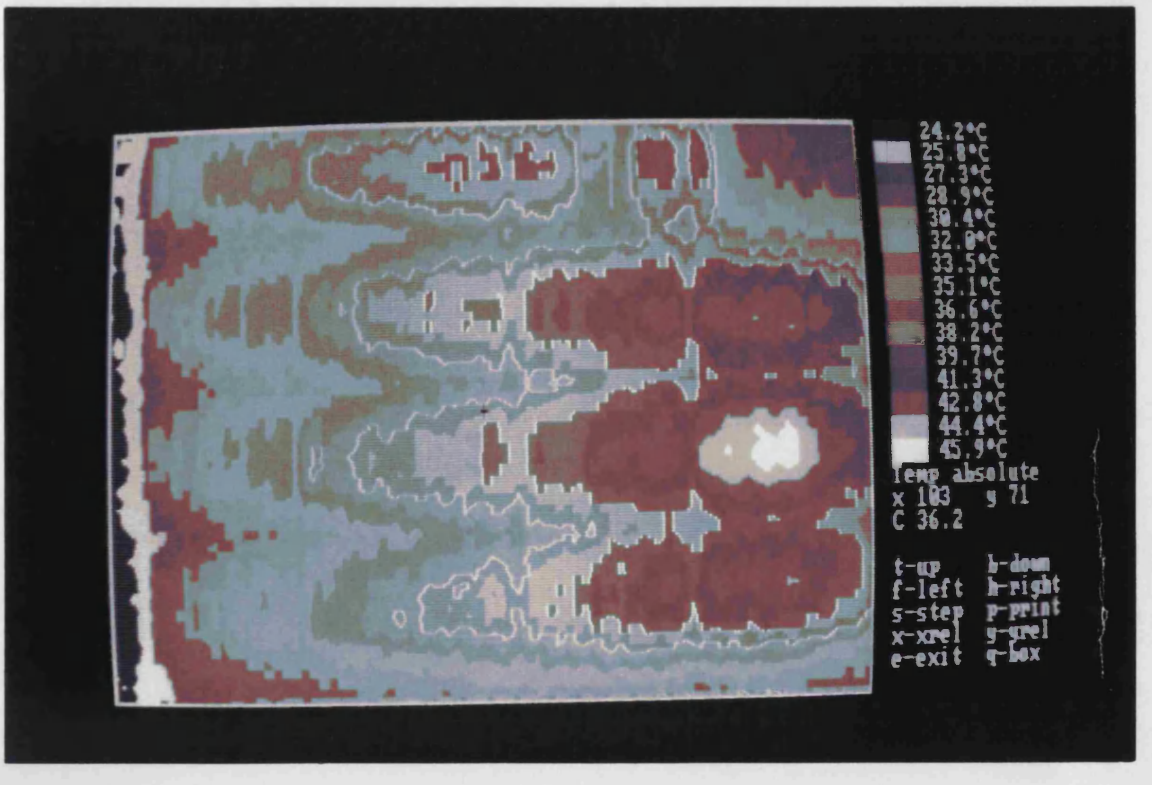


BACK OF THE BOARD

FIGURE 6.13c - THERMAL IMAGE OF THE EURO-CARD
(POWER = 1.2 W/CHIP, V = 5 m/s)



TOP OF THE BOARD



BACK OF THE BOARD

FIGURE 6.14a
COMPARISON OF IR & THERMISTOR TEMPERATURE
UNIFORM POWERING 1.2 W/CHIP VELOCITY 2.5 M/S

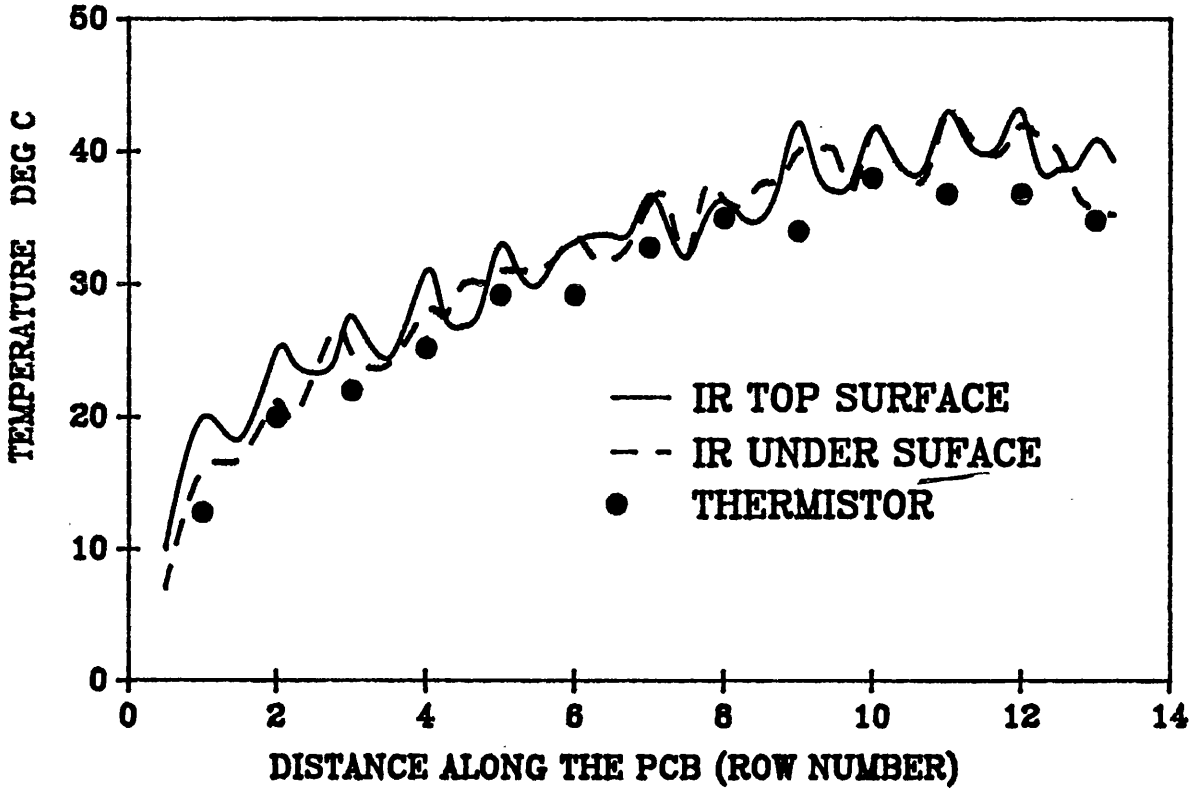


FIGURE 6.14b
COMPARISON OF IR & THERMISTOR TEMPERATURE
UNIFORM POWERING 1.2 W/CHIP VELOCITY 3.8 M/S

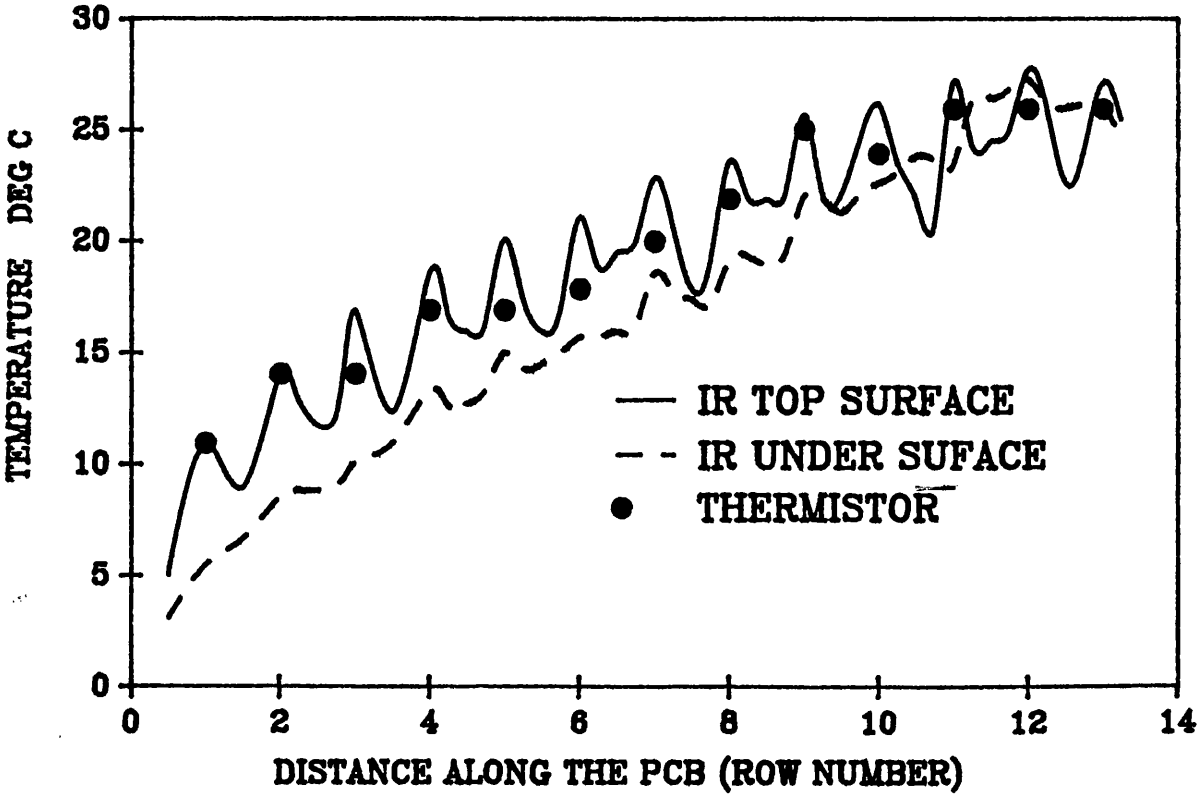


FIGURE 6.14c
COMPARISON OF IR & THERMISTOR TEMPERATURE
UNIFORM POWERING 1.2 W/CHIP VELOCITY 5 M/S

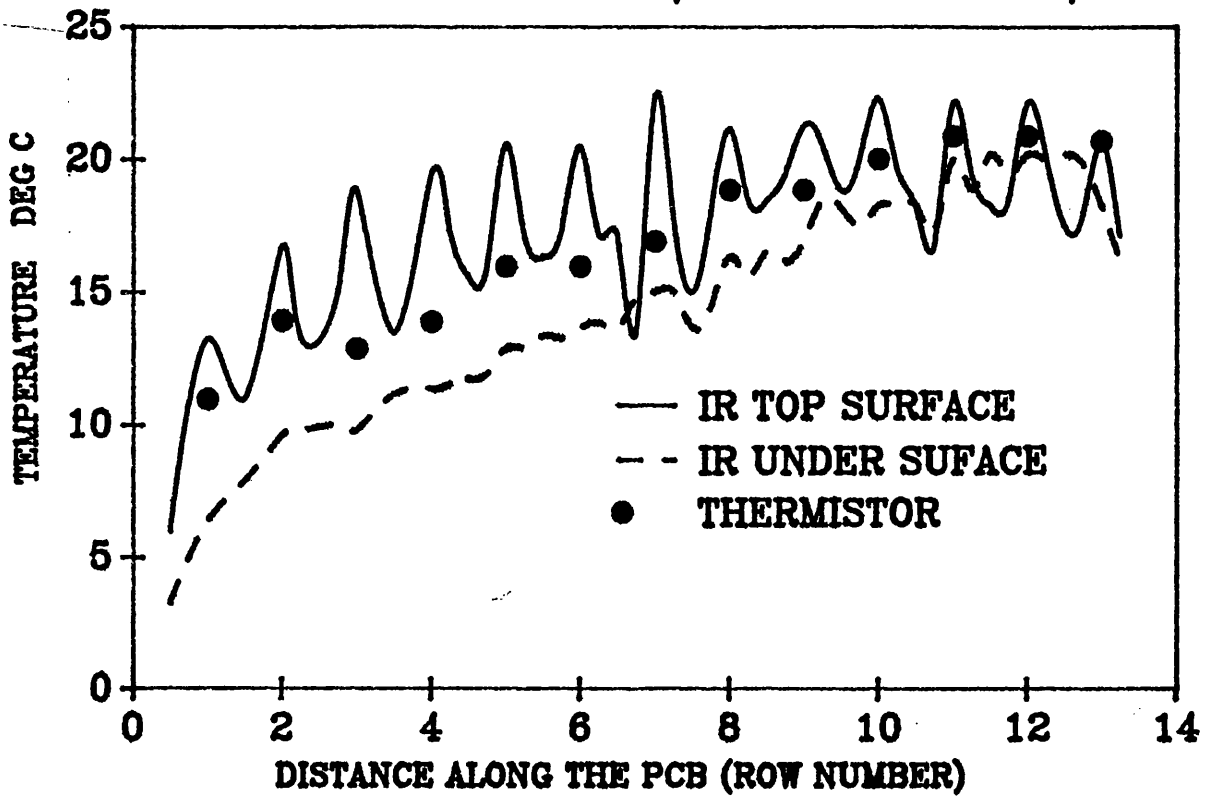


FIGURE 6.15a
COMPARISON OF THE ORIGINAL FE MODEL AND THERMISTOR6
UNIFORM POWERING 1.2 W/CHIP VELOCITY 3.8 M/S

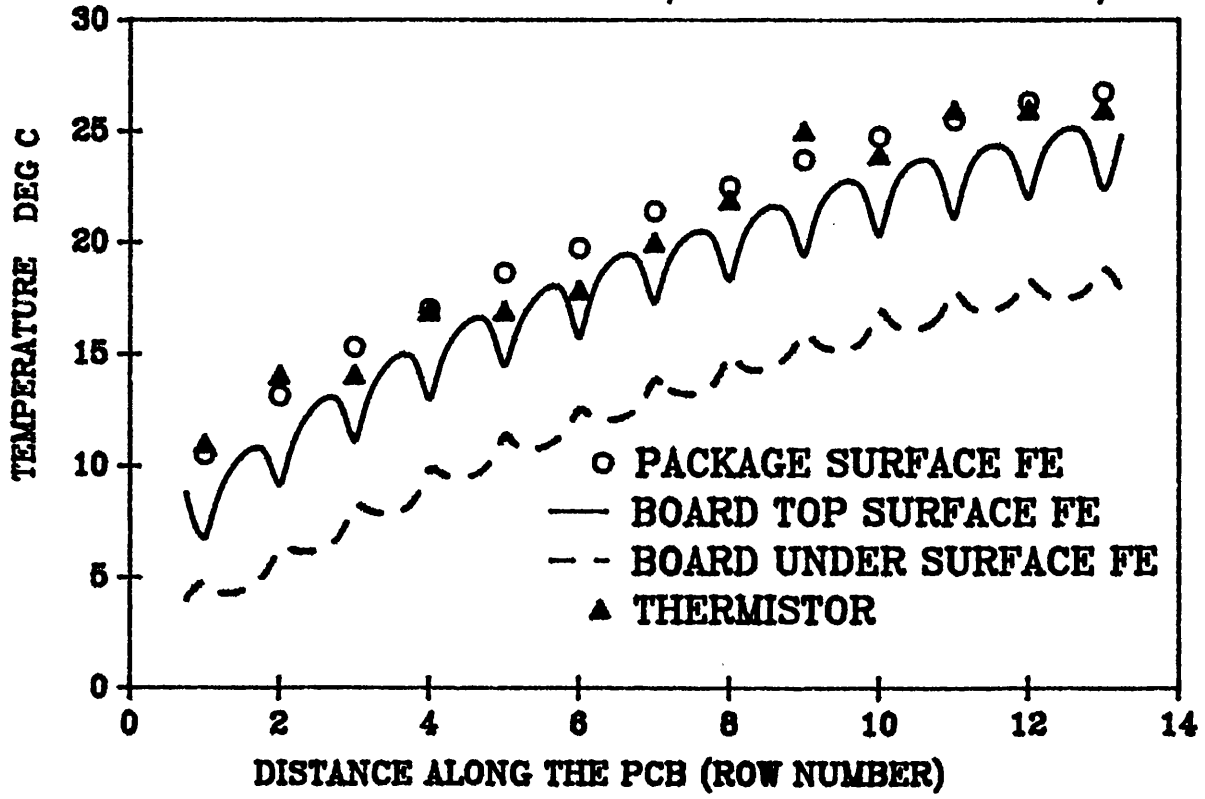


FIGURE 6.15b

COMPARISON OF THE ORIGINAL FE MODEL AND IR IMAGE
UNIFORM POWERING 1.2 W/CHIP VELOCITY 3.8 M/S

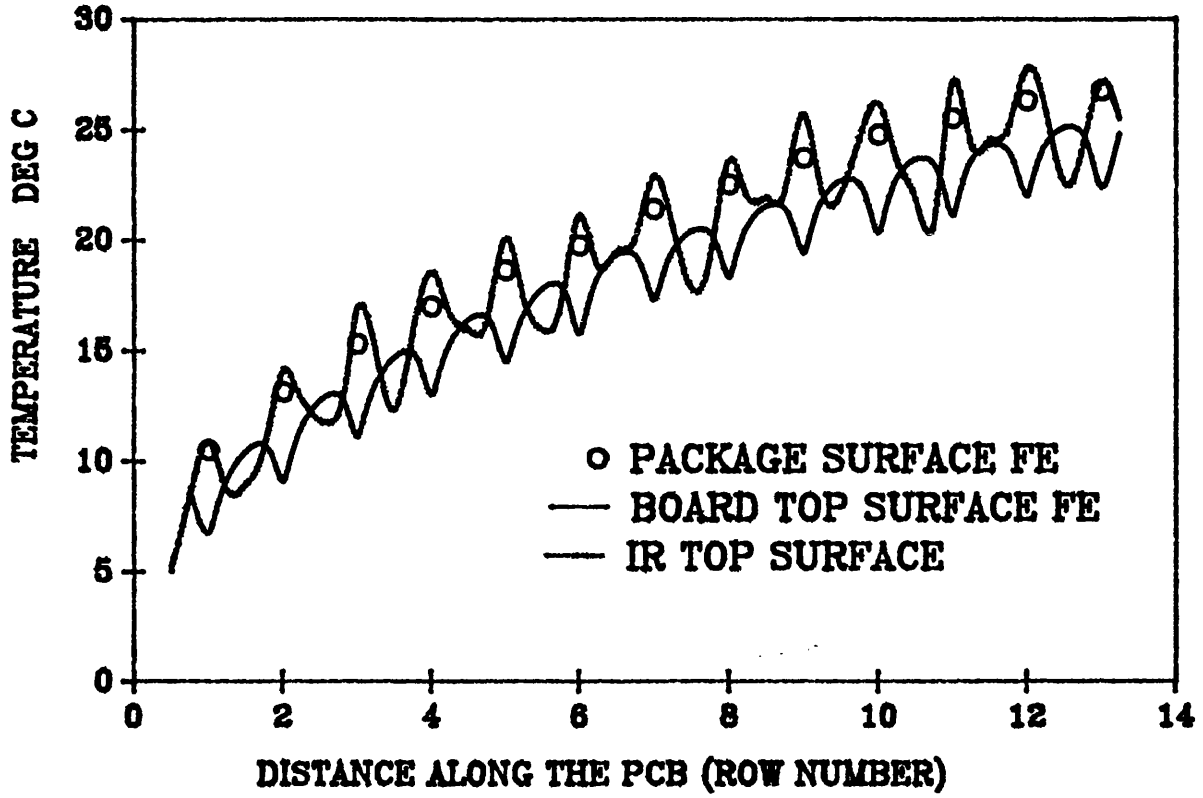
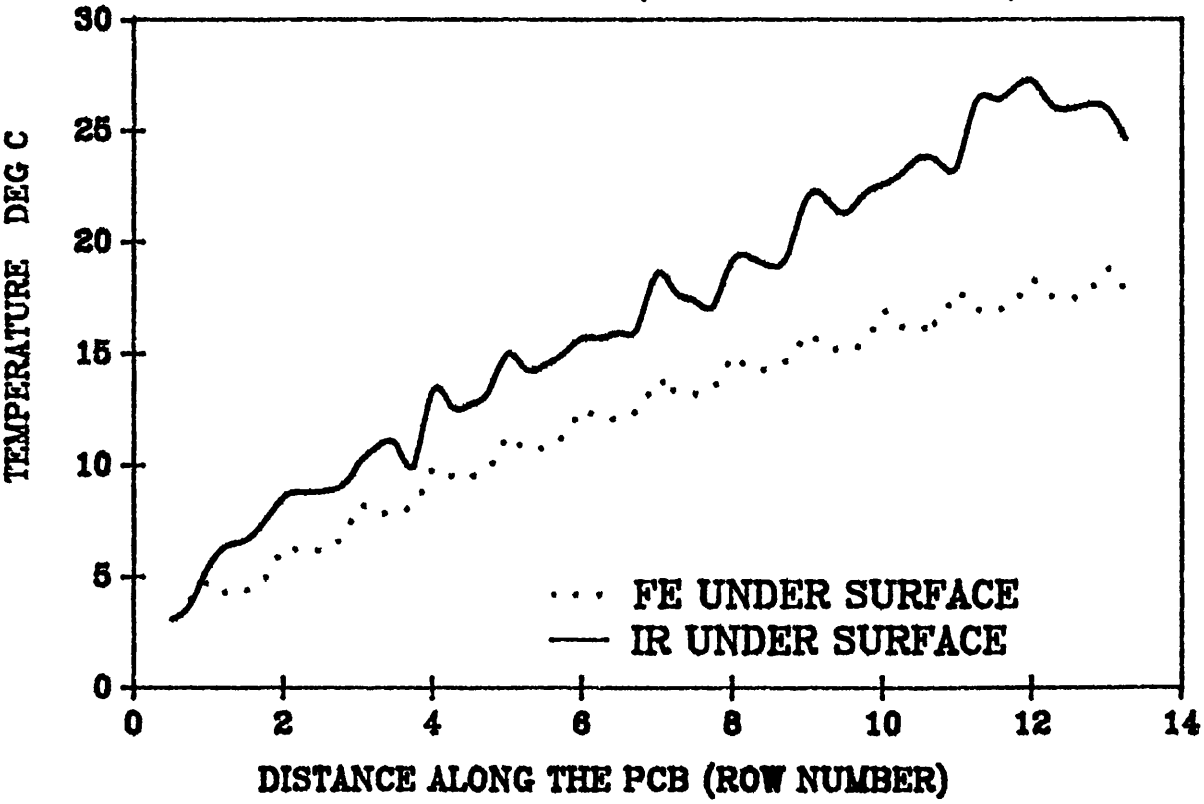


FIGURE 6.15c

COMPARISON OF THE ORIGINAL FE MODEL AND IR IMAGE
UNIFORM POWERING 1.2 W/CHIP VELOCITY 3.8 M/S



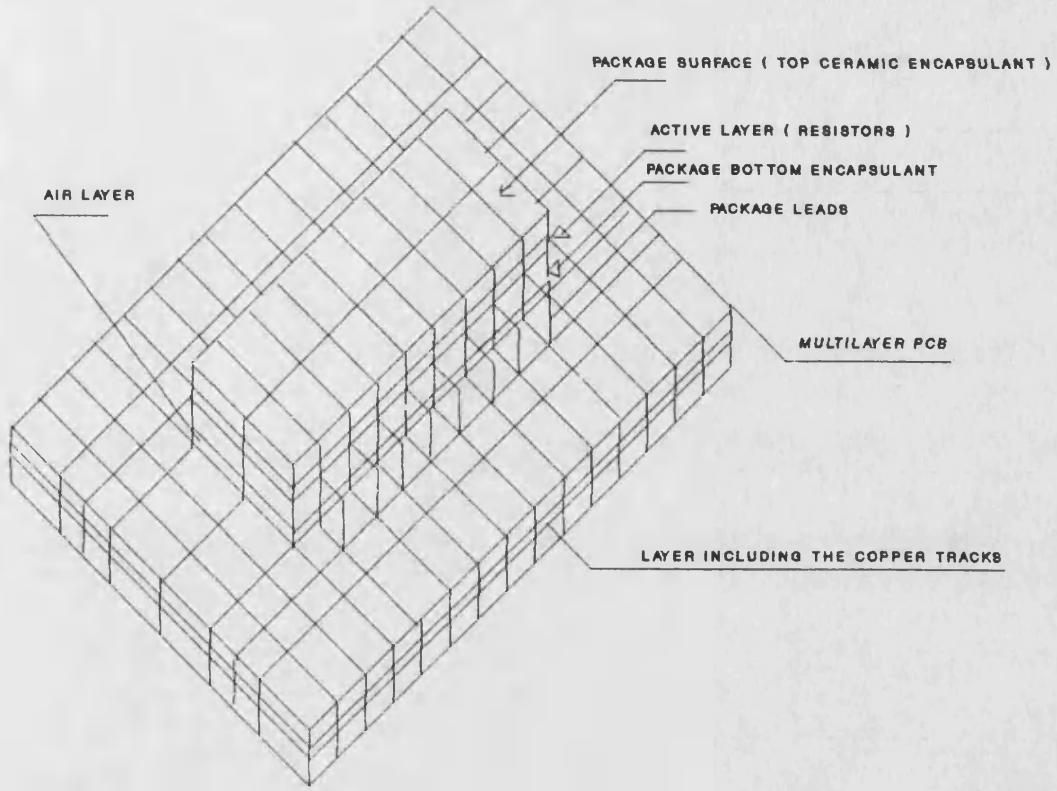


FIGURE 6.16a - MODIFIED FE MODEL

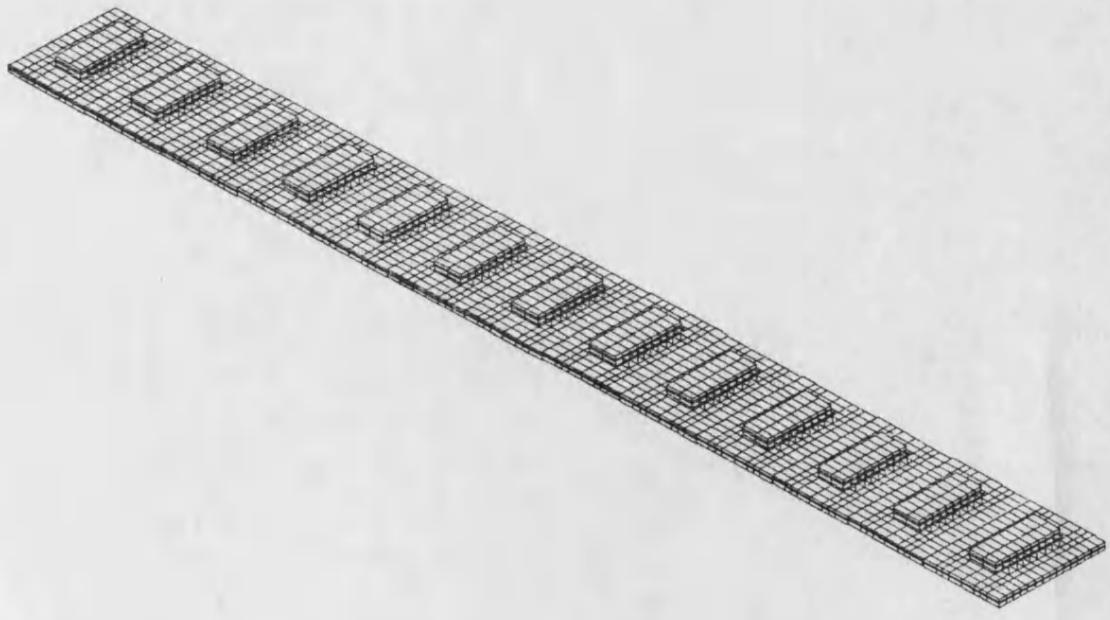


FIGURE 6.16b - FINITE ELEMENT MODEL OF 13 MODULES IN ONE ROW

FIGURE 6.17a

COMPARISON OF MODIFIED FE MODEL AND IR IMAGE VARIABLE
h . UNIFORM POWERING 1.2 W/CHIP VELOCITY 3.8 M/S

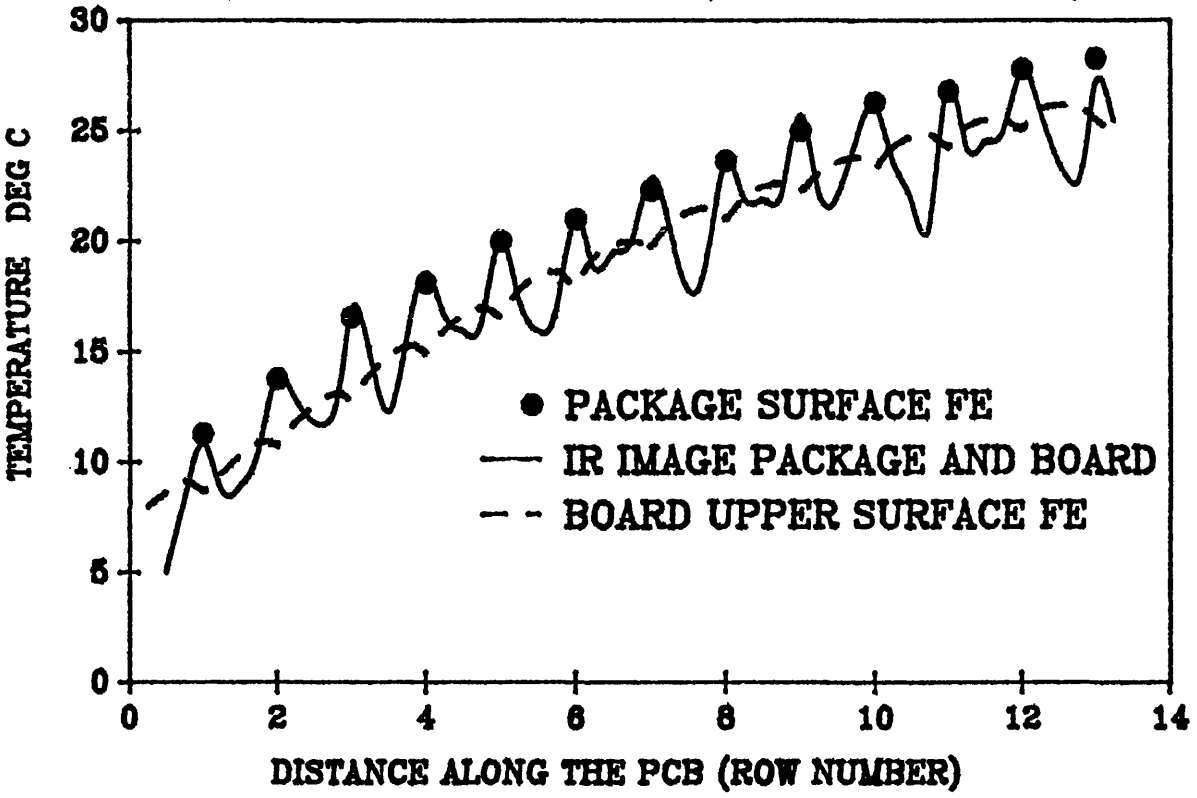


FIGURE 6.17b

COMPARISON OF MODIFIED FE MODEL AND IR IMAGE VARIABLE
h. UNIFORM POWERING 1.2 W/CHIP VELOCITY 3.8 M/S

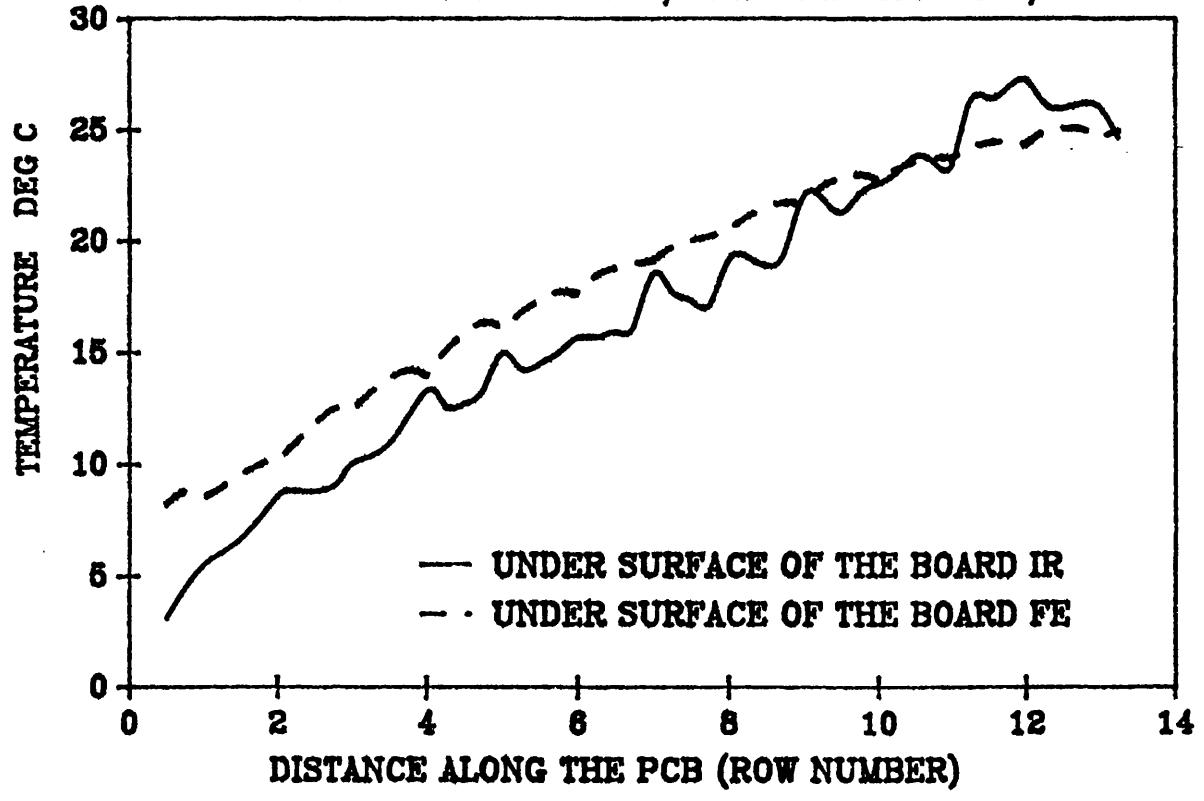


FIGURE 6.18a

IR TEMPERATURE RISE AND EXPERIMENTALLY DRIVED THERMAL WAKE UNIFORM POWERING 1.2 W/CHIP VELOCITY 2.5 M/S

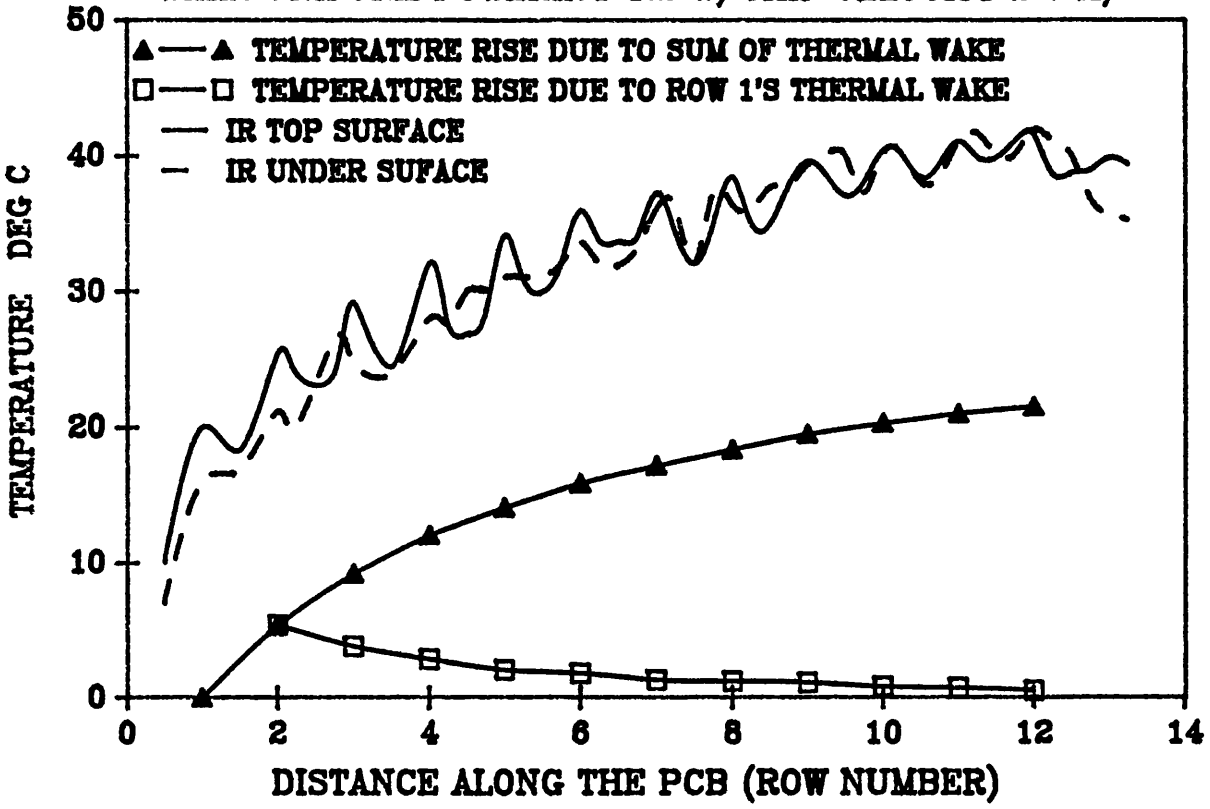


FIGURE 6.18b

IR AND FE TEMPERATURE RISE UNIFORM POWERING 1.2 W/CHIP VELOCITY 2.5 M/S VARIABLE h.

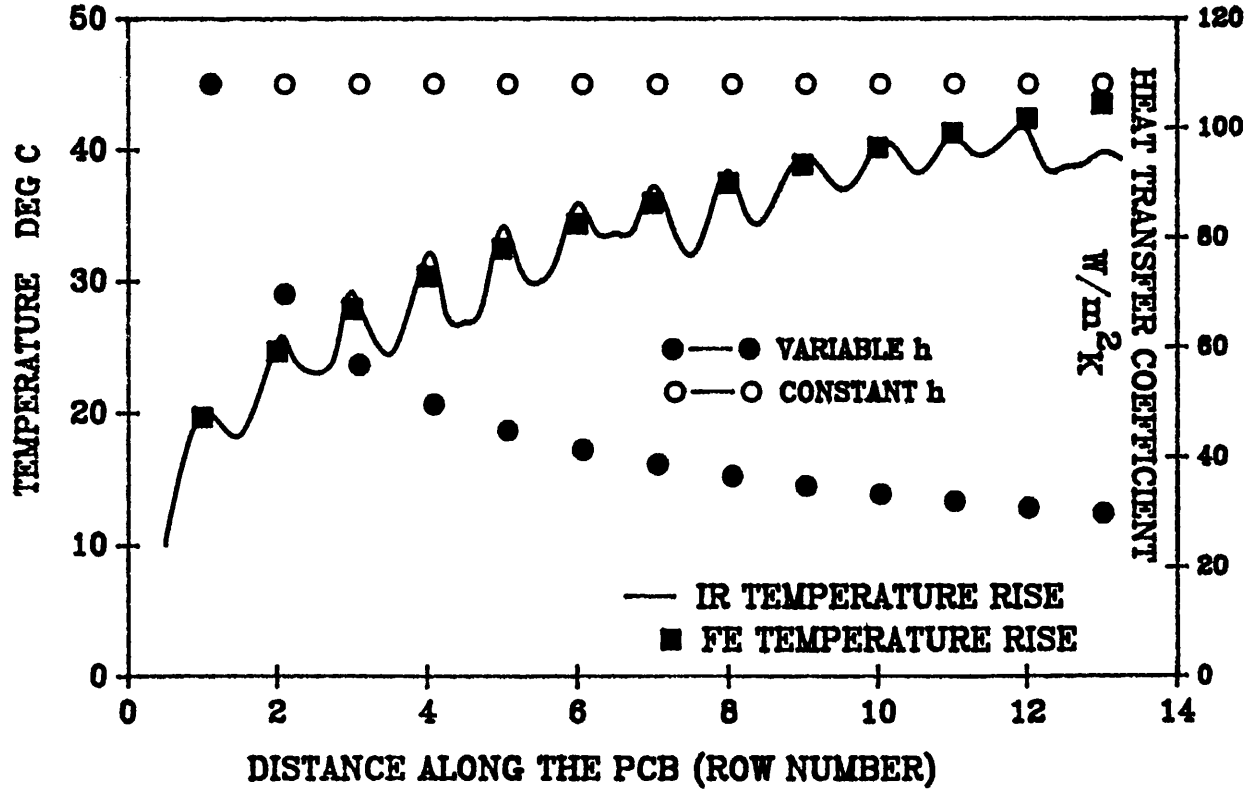


FIGURE 6.19a

COMPARISON OF THE MODIFIED FE PREDICTIONS AND THERMISTOR USING CONSTANT H VALUE AND INFLUANCE COEFFICIENTS UNIFORM POWERING 1.2 W/CHIP VEL. 3.8 M/S

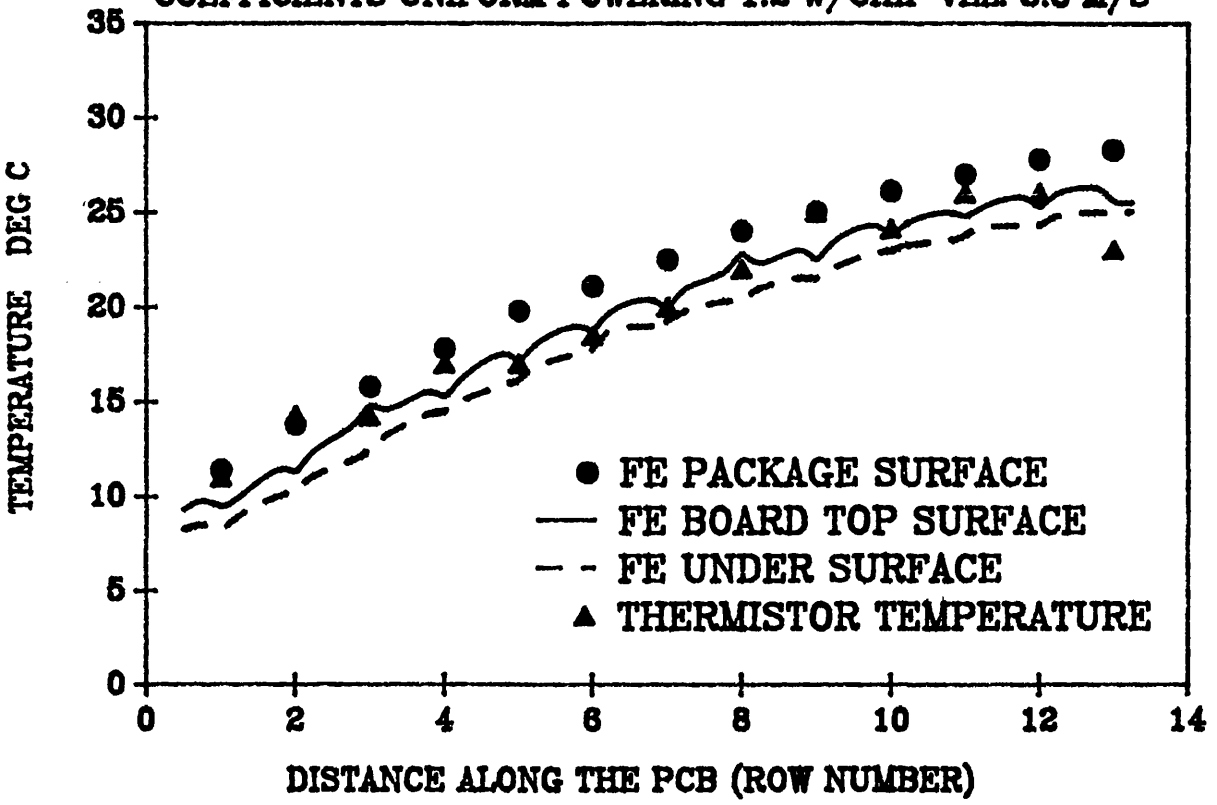


FIGURE 6.19b

COMPARISON OF THE MODIFIED FE PREDICTIONS AND IR USING CONSTANT h VALUE AND INFLUANCE COEFFICIENTS UNIFORM POWERING 1.2 W/CHIP VEL. 3.8 M/S

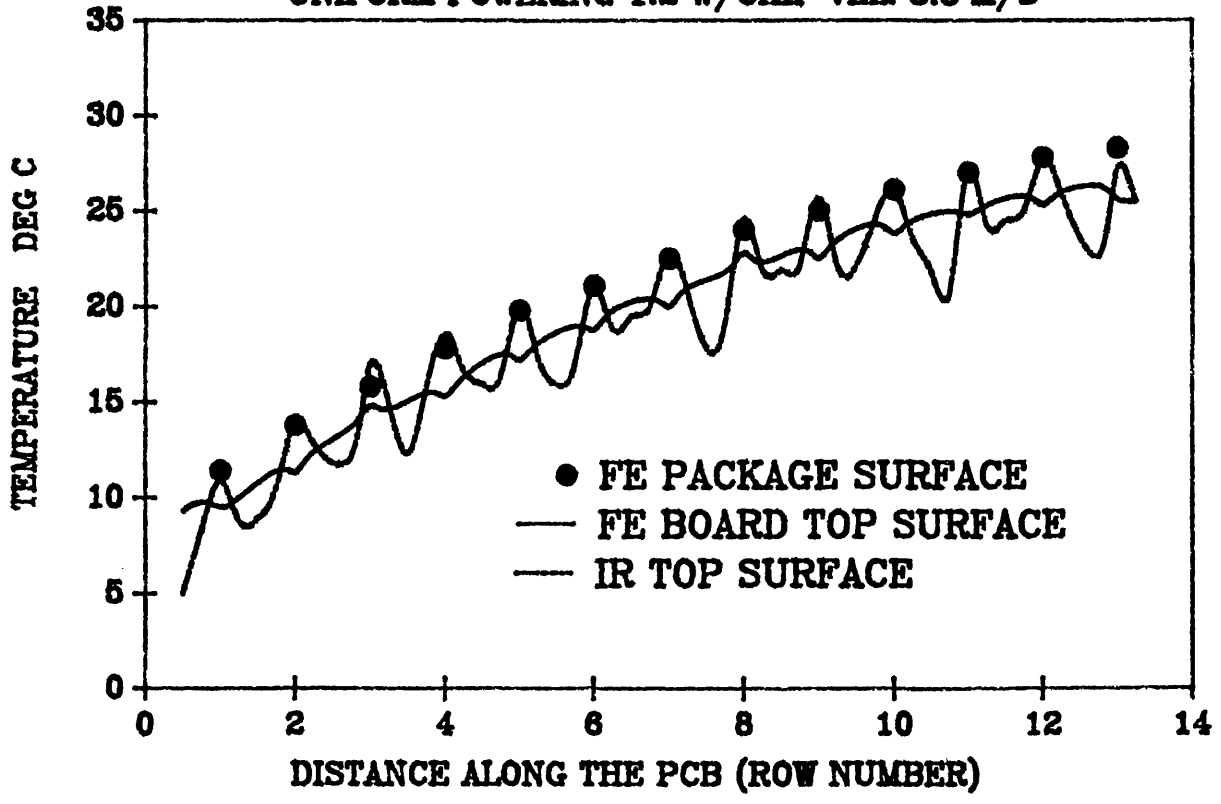
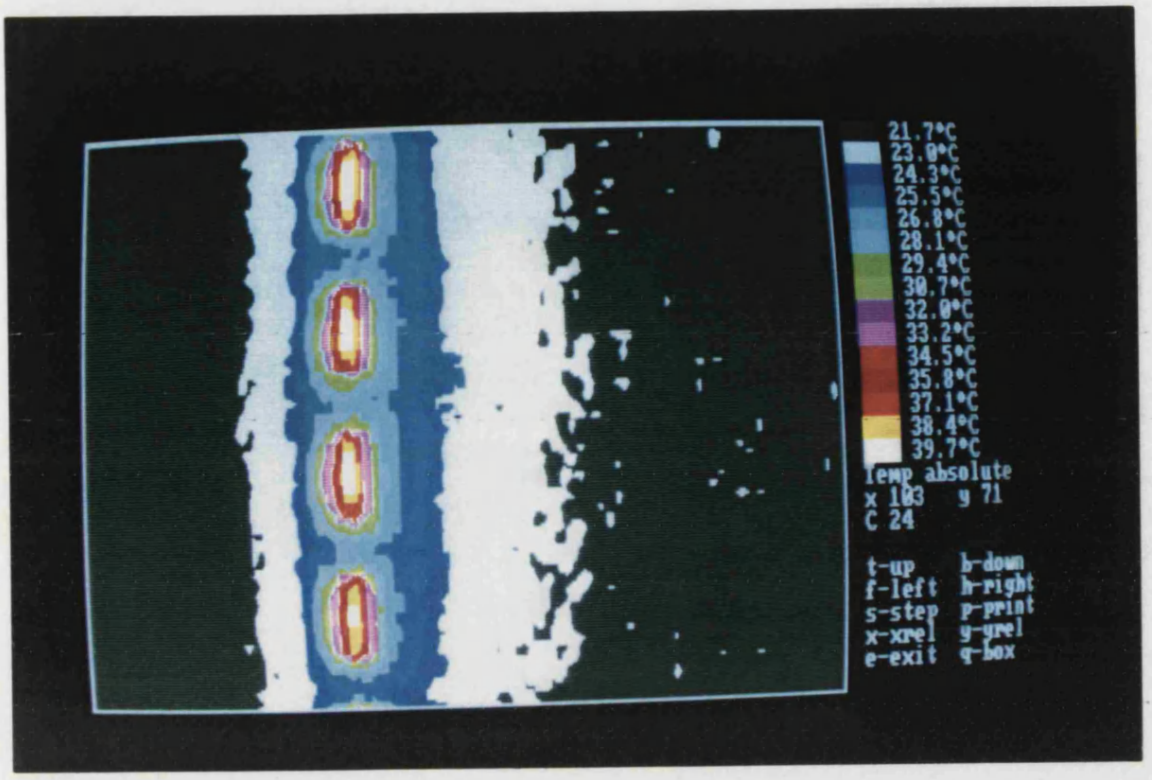


FIGURE 6.20 - THERMAL IMAGE OF THE EURO-CARD
ROW 5 POWERED
(POWER = 1.2 W/ CHIP, V = 2.5 m/s)



TOP OF THE BOARD

BACK OF THE BAORD

FIGURE 6.21a

COMPARISON OF IR AND THERMISTOR NON-UNIFORM POWERING (ROW 5) 1.2 W/CHIP VELOCITY 2.5 M/S

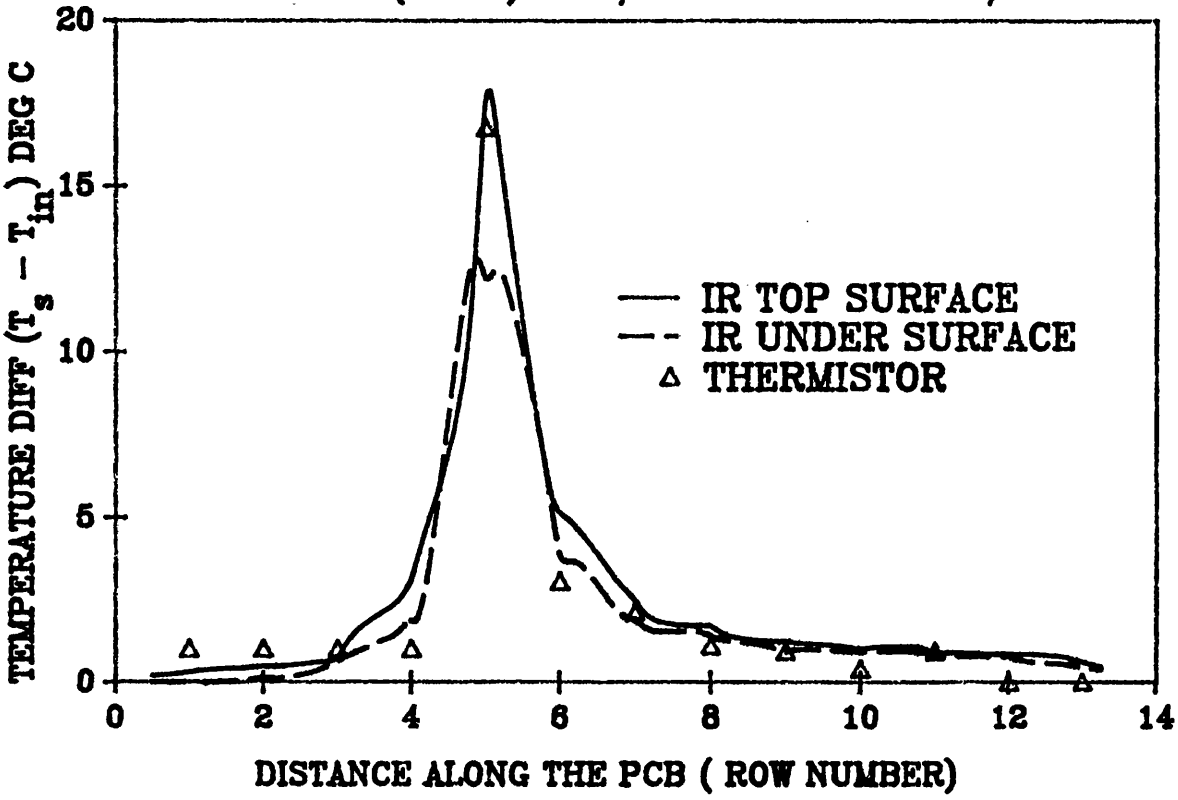


FIGURE 6.21b

COMPARISON OF IR AND THERMISTOR NON-UNIFORM POWERING (ROW 5) 1.2 W/CHIP VELOCITY 3.8 M/S

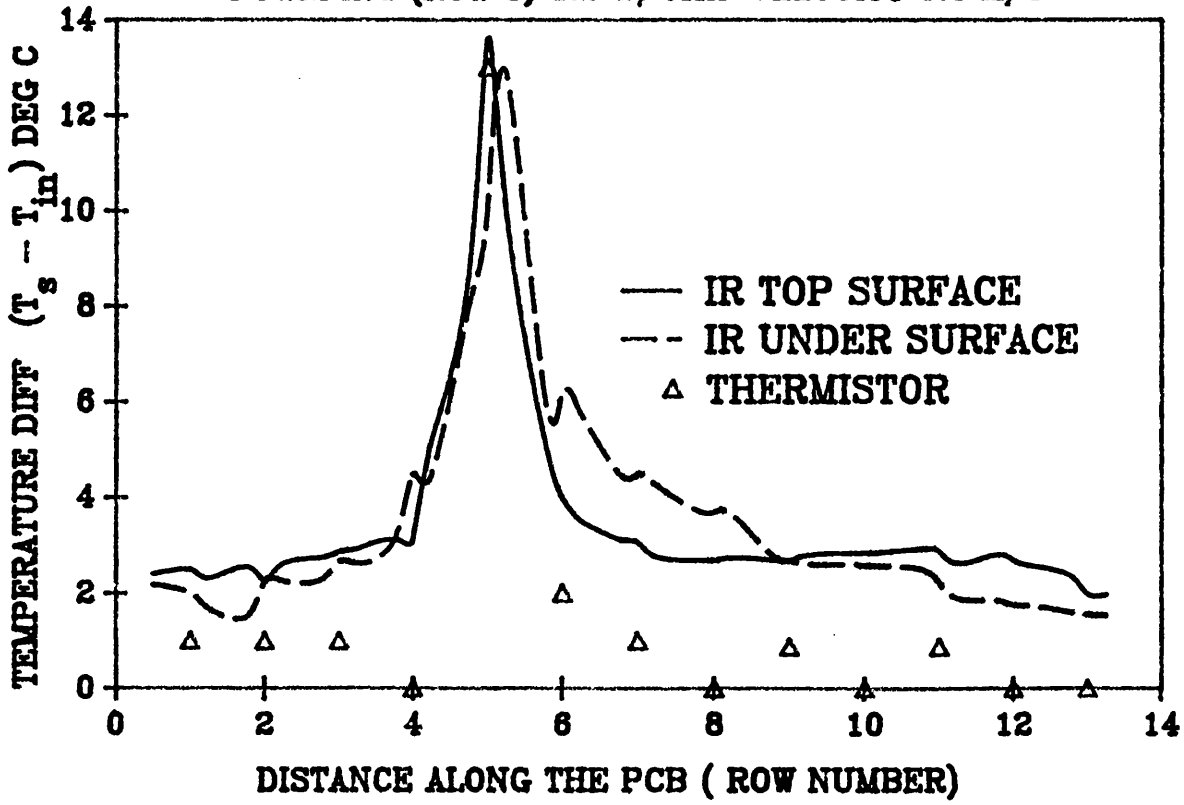


FIGURE 6.22a

COMPARISON OF THERMISTOR AND MODIFIED FE MODEL
h. AND INFLUANCE COEFFICIENT CONSTANT NON UNIFORM
POWERING (ROW 5) 1.2 W/CHIP VELOCITY 3.8 M/S

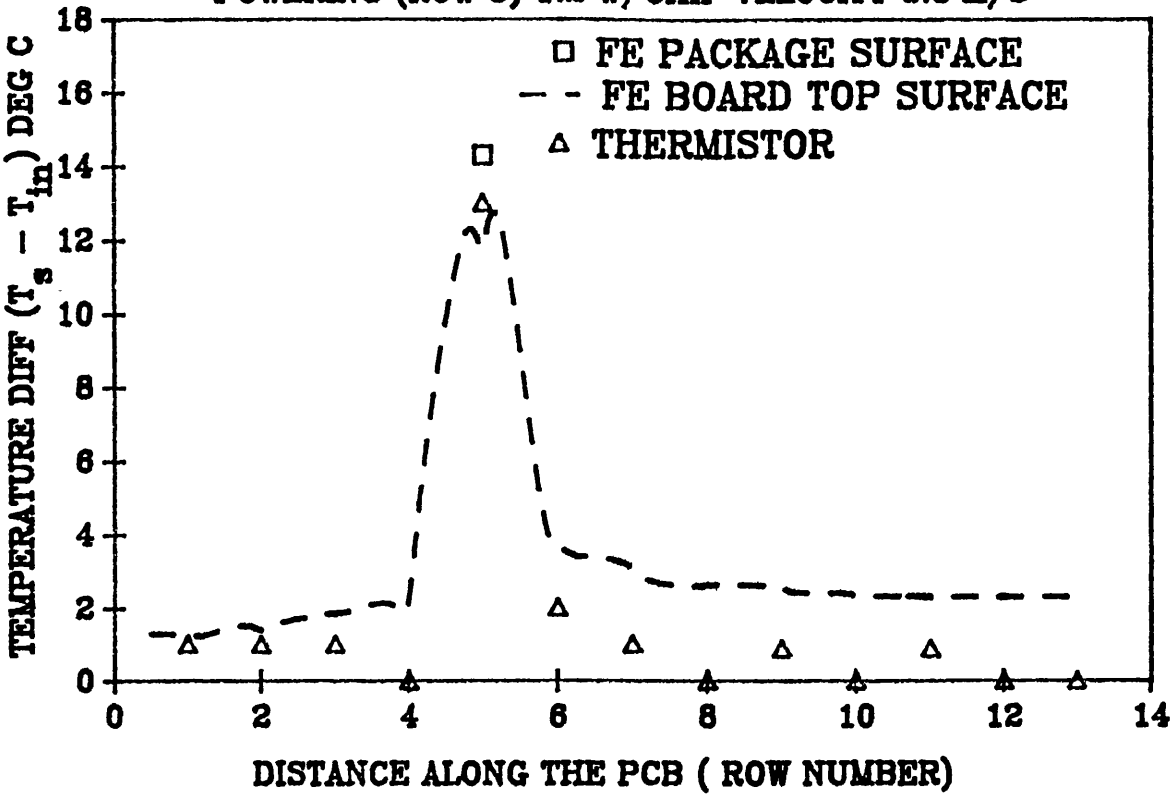
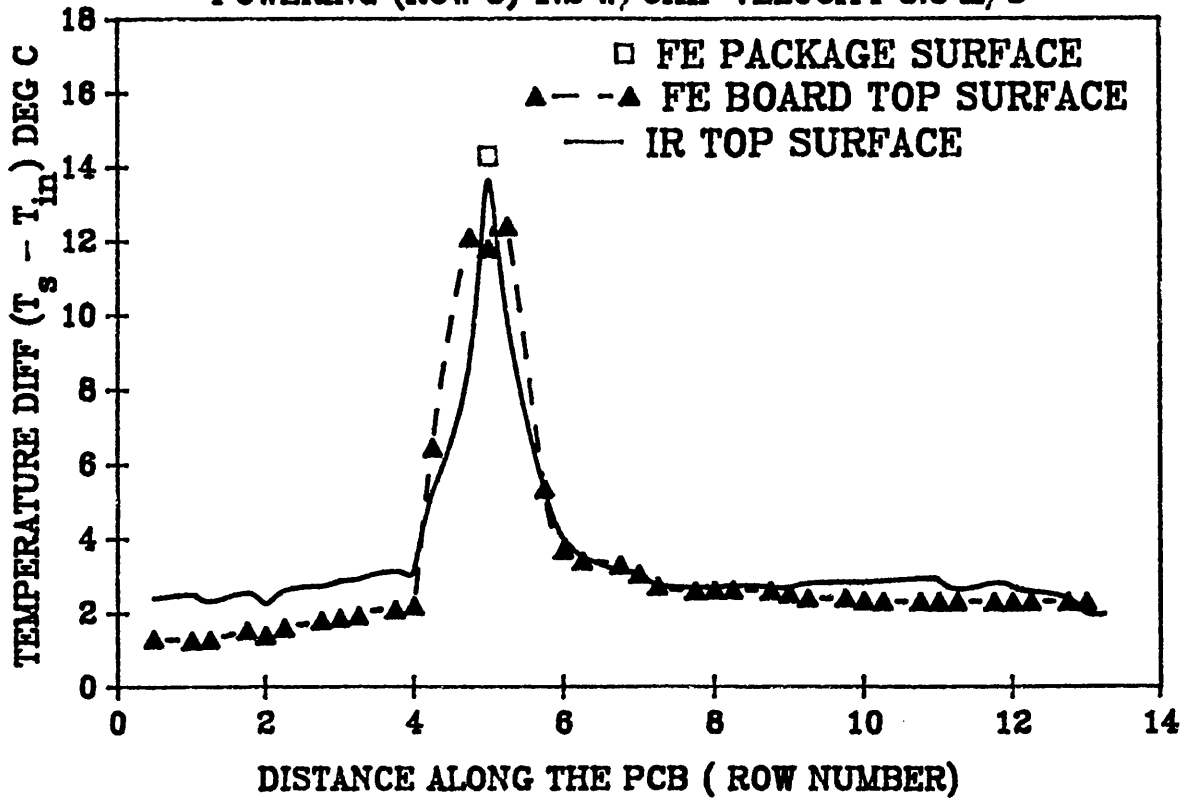


FIGURE 6.22b

COMPARISON OF IR AND MODIFIED FE MODEL CONSTANT
h. AND INFLUANCE COEFFICIENT NON UNIFORM POWER
POWERING (ROW 5) 1.2 W/CHIP VELOCITY 3.8 M/S



CHAPTER 7

EXPERIMENTAL INVESTIGATION OF FORCED CONVECTION COOLING OF SURFACE MOUNTED COMPONENTS

7.1 INTRODUCTION

Designers of VLSI (very large scale integration) continue to strive for ever decreasing feature sizes and the corresponding increase in functional integration at the chip level which these afford. A parallel effort in the packaging arena has spawned the evolution of a relatively new family of plastic and ceramic surface mount components, which are mounted directly on the surface of the substrate. These new schemes of packaging and interconnection, almost without exception, will require more stringent control of the thermal environment. Furthermore it is to be noted that in this type of device, the geometry of the heat conduction paths and coolant paths is dictated by the arrangement of the electronic circuits and internal leadframe. It is with the low I/O count (20 pin) member of this family that this part of research is concerned. The terms plastic leaded chip carrier (PLCC) and ceramic leaded chip carrier have been loosely applied to those surface mounted constructions which, by virtue of their thin bodies and "J" leads result in a very low profile package.

A program of experimental research accompanied by finite element modelling was under taken to accomplish the thermal control problems associated with an array of

PLCC packages mounted on a custom made PCB (thermal test board).

For the purpose of FE modelling, the thermal conductivity of the plastic encapsulant had to be determined. This proved difficult, because manufacturers, depending on their design, load the plastic with "filler" material to achieve a particular value of thermal coefficient of expansion. Their objective is to match the expansion coefficients of package and substrate to minimize if not totally eliminate thermal stress.

The method adopted to establish the thermal conductivity of the plastic molding, was the combined use of FE modelling and infra-red surface temperature measurement. This was feasible, because the infra-red scanner described in Chapter 6 could be made to scan the actual coordinates associated with the nodal orientation of the FE model.

To evaluate a heat transfer correlation based on the bulk fluid temperature (T_{bulk}) for the thermal test board, experimental data were collected in the form of a thermal image, from which, the temperature distribution along the pcb was extracted using the image processing software described in Chapter 6. The test section was horizontally mounted in a rectangular channel and the forced convective airflow was hydrodynamically fully developed. The SID pulsing board described in Chapter 4 was employed to sense chip junction temperatures. A comparative series of tests was carried out using air velocities in the range 1.6 to 8 m/s and chip power dissipations in the range 0.5 to 2 W. Values of internal thermal resistance of the package, and of heat transfer coefficients for these tests are presented.

7.1.1 DESCRIPTION OF THE SURFACE MOUNT PACKAGE (PLCC)

Figure 7.9 shows construction details of PLCC. The device is bonded to an alloy 42 leadframe with silver-filled polyimide adhesive. The structure is then transfer molded with novolac molding compound.

The PLCC was developed by Texas Instruments in 1980 to improve packaging density of IC's on PCB's and overcome some of the size and mounting arrangement constraints caused by DIP packages. The PLCC was also designed to be used under the same environmental conditions as the DIP without any reliability degradation. The PLCC occupies approximately 40% to 60% of the PCB area of an equivalent DIP and because it is attached to the surface requires no through holes. The design of the lead provides compliance allowing the use of any commercial substrate. Devices are offered in 18, 20, 28, 44, 52, 68, and 84 pin packages. A typical PLCC package is illustrated in Figure 7.1a, and corresponding thermal data are shown in Figure 7.1b.

7.1.2 RELEVANT LITERATURE

A comprehensive literature search revealed few publications on the thermal analysis of surface mount systems. Moreover these publications indicated that the majority of heat transfer problems of such packages have not as yet been solved satisfactorily. Under these circumstances, this part of the research cannot provide a precise summary of what has been done, and what appears to lie ahead in the area of heat transfer research related to surface mount devices. However a few references to heat transfer

studies of other types of SMC (surface mount component) or simulation of the SMC will be undertaken.

Recent research in forced convection of SMC's has addressed almost exclusively the cooling of heat sources related to two packaging configurations:

a) Chips packaged in rectangular modules that are mounted along or in an arrays on a PCB.

b) Direct liquid cooling of bare heat-dissipating chips mounted on a multilayer ceramic substrate.

Nakayama [76] has presented a concise review of current technology, including the description of state-of-the-art packaging technology. The review shows the primary components of a chip-in-cavity packaged with heat sink attached. A description of air cooling of such packages is also given. Bar-Cohen (1985) [77] critically reviewed those various thermal packaging technologies used, in state-of-the art- electronic systems.

Forced convection liquid cooling from flush-mounted rectangular sources was examined by Samant and Simon [78]. In these studies either water or a coolant such as R113, FC72, FC77 was employed as the working fluid.

Ramadhyani, Moffatt, and Incropera have preformed numerical studies of conjugate heat transfer from one or more two-dimensional flush strip heaters on the floor of a channel with fully developed laminar [79] or turbulent [80] flow. The results of this

investigation were compared to data from single square sources, and from an array of twelve such sources in water and FC77. Their results are presented in terms of the average Nusselt number (defined in terms of the heat flux from the heater only and the channel hydraulic diameter) over a single source in laminar flow, normalized by the value for an adiabatic substrate. They demonstrated that the substrate conduction decreased the average Nusselt number over the source and was especially significant at low Peclet number. The reported data for turbulent flow [80], using a standard eddy-diffusivity closure model, were consistent with turbulent flow, however the magnitude of the Nusselt number reported is much greater and substrate conduction reduced.

Forced and natural convection experimental studies was carried out by Furkay [81] on plastic and ceramic flat packs devices respectively. Also two dimensional and three dimensional FE simulations were presented to determine the effects of changes in material and parametric variation in geometry on package thermal performance. Comparisons with empirical data were made where possible. The study was however limited to single packages and the associated small section of the epoxy PCB. No data are reported of the thermal interaction between neighbouring packages. For natural convection tests, the packages were placed in a vertical channel. A custom made thermal test chip was used to simulate the device power and to sense the bulk chip temperature.

Alli, Mahalingam and Andrews [82] investigated the thermal characteristics of one class of surface mount packages, namely, small outline transistor 23 and 89 packages.

Experimental thermal resistance data for single component plastic SOT-23 AND SOT-89 packages were reported. They used a commercially available infra-red thermal imaging camera, together with an electrical parameter to determine the thermal resistance of the device. The most noteworthy observation reported is that the external thermal resistance is about 2/3 of the overall thermal resistance and thus controls the package thermal behaviour. The effect of density of mounting on thermal resistance is reported using the IR technique. The authors also report the effect of variation of package pitch, relative orientation of neighbouring packages, and one-sided versus double-sided mounting arrangement. Although the subject of electrical parameter modelling, and IR technique were mentioned no details of either techniques were given.

The work under taken in this part of the research was intended to complement existing work and provide more data about the complex heat transfer processes involved in the forced convection cooling of the surface mounted components.

7.2 OBJECTIVES

The main objectives of this part of the research are as follows:-

1) Choosing a surface mount device suitable for research.

2) The design and manufacture of a thermal test board housing an array of surface mount devices, with specific arrangements to facilitate Junction temperature measurement using SID.

3) To design and build a test rig suitable for heat transfer measurements on the thermal test board, incorporating the SID and IR scanning unit.

4) To modify the existing data acquisition system to enable automatic powering (both uniform and non-uniform) of the thermal test board.

5) To measure typical temperature distributions and record thermal images of the components along the thermal test board, at varying air velocities and power configurations.

6) To establish the thermal conductivity of the plastic encapsulant using the combined FE model and infra-red surface temperature technique, and validate the method with suitable experiments.

7) To investigate the thermal boundary layer and the film heat transfer coefficients based on the bulk mean fluid temperature, along the PCB under uniform powering conditions. This would require development of detailed finite element model of the thermal test board. Finally experimental data from the test rig was to be compared with predictions from the FE model.

7.3 RIG ASSEMBLY AND GENERAL DESCRIPTION

The experimental test rig was configured similar to the rig described in Chapters 3 and 6. The major difference was in the test and dummy section. The test PCB and the dummy boards were set in line by gluing a strip of perspex (5mm thick) to the under surface of the adjoining PCBs. This arrangement prevented the formation of fully developed boundary layer on the bottom of the board, whilst ensuring the formation of a fully developed hydrodynamic boundary layer on the top surface. The rig was also designed to have sufficient flexibility so that various board configurations could be tested. Provisions were made to allow variations in geometry, heat dissipation pattern as well as variable airflow rates.

Figure 7.2a shows block diagram of the main components of the test rig assembly which can be summarised as follows:-

1) ***Additional mechanical components and instrumentation***

(a) Pitot tube, flow meter.

(b) Instrumented thermal test board.

2) ***Electronic control system***

(a) SID pulsing board.

(b) Modified interface unit.

A schematic of the test rig showing all components is illustrated in Figure 7.2b.

7.3.1 TEST RIG MECHANICAL COMPONENT ARRANGEMENT

The dummy section consisted of a honeycomb flow straightener and two PCBs identical to the thermal test board un-powered Figure 7.2b. The dummy boards provided a well defined reproducible hydrodynamic fully developed flow upstream of the test pcb on the top surface. The dummy boards used were also capable of being powered to the same level as the test PCB if required.

The inlet free length of the duct was designed such that it was three times that of the exit free length. This provided an equally well defined and reproducible flow patterns at the first and last row of the components in the duct. The test section houses an instrumented PCB supported by the wooden wall and the duct side wall lid, Figure 7.3 and photo Figure 7.4.

7.3.2 TEMPERATURE AND AIR FLOW MEASUREMENTS

The surface and junction temperature measurements were similar to that described in chapter 6 and 4 respectively.

The total air volume flow rate was measured in a manner similar to the described in section 3.5 of chapter 3. In addition to the pressure drop measurements across the orifice plate, two new pressure measurements were carried out.

A pitot tube and a flow meter was placed down stream of the thermal test board before the diffuser. This section of the rig was designed so that the pitot tube and flow meter could be moved in a vertical direction. This allowed measurement of the air velocity as it left the test board. This value was then checked against the orifice plate measurements.

7.3.3 ELECTRONIC DATA ACQUISITION SYSTEM

A description of the data acquisition system was given in Chapter 3, The same configuration of the ADU was used in this part of the research with an alteration to the OP-AMP MULTIPLEXING CARD.

The OP-AMP MULTIPLEXING CARD was used to relay signals from the ADU 16 ADC (analog to digital converter) channel as follows:

a) Eight lines to the OP-AMP cards, each line was used to power a group of four

surface mount component on the thermal test board. The power configuration was controlled by a newly designed interchangeable patching (standard Euro-card edge connector) plug, which was wire wound in such a manner to power each row of SMC's individually. The flexibility of the patching plug designed allows any required power configuration to be achieved. The rest of the OP-AMP MULTIPLEXING CARD was adequately configured and was kept the same Figure 7.5.

7.4. SELECTION OF A SURFACE MOUNT DEVICE FOR THE TEST BOARD

After a careful search the PLCC device chosen for the thermal test board was the PLCC SN72501FN. This device is a 20 pin military package manufactured by Texas Instrument to facilitate the evaluation of thermal performance. The device consists of a series resistor networks which is protected by a transistor from the sudden reversible of current, Figure 7.6. In this device the temperature sensitive parameter (TSP) is a transistor. The base emitter diode could be forward biased by the pulsing board described in Chapter 4, and the resultant V_{be} (base emitter voltage) value is then indicator of the junction temperature.

7.5 DESIGN AND MANUFACTURE OF THE THERMAL TEST BOARD

7.5.1 DESIGN PROBLEM

The main PCB design problems were identified as follows:

1) Control of power dissipation.

2) Measurement of SID output voltage (temperature of junction).

3) Positioning of thermistor on board.

4) Data acquisition system - (compatibility with the existing DAU)

7.5.2 COPPER TRACK ART WORK ON PCB

In an attempt to alleviate the assumptions and problems experienced in the modelling of a multilayer heterogeneous PCB (standard Euro-Card) described in Chapters 3 and 6, it was decided that the custom made PCB should have a simple homogenous construction. This involved spending a lot of effort and time in designing a small number of copper tracks which were as fine as possible.

i) ***Thermistors***

It was decided to construct the PCB from a single layer of laminated epoxy these greatly facilitated FE modelling. Although the surface temperature measurements were to be carried out using the infra-red scanning equipment, a total of fourteen miniature surface mounted thermocouples were positioned on the PCB to verify IR data. The arrangement of the thermistors and, the layout of the associated corresponding copper tracks are illustrated in Figure 7.7a.

ii) *SID*

The transistors (base emitter) in each device which provides the SID measurement, are grouped in sets of four with a common ground, and are terminated on the top surface of the PCB in form of a rivetted hole through to the back of the PCB, where the copper tracks are extended to the two 64 way edge connectors Figure 7.7b.

iii) ***Power supply***

With reference to Figure 7.6, the power dissipation for each device was determined and measured through the voltage drop across the common resistor network utilising a total of 200 Ω +/- 20%. The copper track from the device to the edge connector was set out on the top surface of the PCB as shown in Figure 7.7c

7.5.3 DEVICE LAYOUT ON PCB

The layout of the devices mounted on the test board is shown in Figure 7.8. The size of the PCB was governed by the number of packages on the board, their pitch and the size of the two edge connectors. From the final detailed drawing a specialist in the custom-manufacture of PCBs (external to the university) was able to manufacture the final test assembly shown in Figure 7.9.

7.5.4 CALIBRATION OF THE THERMAL TEST BOARD

The calibration of the temperature sensitive parameter of the PLCC was carried out according to the manufacturers data sheet [83]. The emitter base diode was forward biased (as described in chapter 4) at constant current of 1mA as shown in Figure

7.10a, and the resultant V_{BE} value was used as an indicator of the junction temperature at ambient temperature T_{amb}. The thermal test board was then placed in an oven and the temperature of the oven was elevated to 65°C. After temperature stabilisation the resultant V_{BE} was recorded. A plot of V_{BE} vs temperature is shown in Figure 7.10b.

7.6 EXPERIMENTAL PROCEDURE

Tests were performed by uniformly powering the thermal test board via the software [31], through the computer and the mowlem (ADU). After the steady state conditions had been reached (normally within 30 min.), the program (Chapter 6) was initiated to scan the thermal test board in steps of 2mm. The temperature array file written by the scan program was then submitted to the image processing software (chapter 6) to produce a thermal image of the test PCB. Each thermal image was analyzed and a detailed temperature distribution of the middle row on the test board was obtained. Each experimental temperature distributions were matched with the predictions from a detailed FE model of the package and PCB. Tests were performed in the range of (0.5 to 2) watts and varying air speed of (1.6 to 8) m/s.

The particular tests carried out to determine the thermal conductivity of the plastic (which constituted the body of the PLCC) are discussed in detail below.

7.7 DISCUSSION OF RESULTS

7.7.1 GENERAL

The convective heat transfer from a component is usually described in terms of a heat transfer coefficient. The convective heat transfer coefficient is a defined quantity, not a physical one, and its definition involves some subtleties which are not always appreciated.

The heat transfer coefficient, h, is defined as the heat flux from the surface divided by the temperature difference between the surface and the fluid. Significant difficulties in application arises because there is more than one way to define the reference fluid temperature and the numerical value of h, depends on which particular fluid temperature is chosen.

In electronic cooling situation, there are four options for the reference fluid temperature;

1) The adiabatic temperature of the element (T_{ad}).
2) The mixed mean temperature of the air in the channel (T_{bulk}).
3) The inlet temperature (T_{in}).
4) The air temperature far from the element (T_{∞}).

For this channel flow problem, T_{∞}) is difficult to measure, hence option 4 was not practical. The other three options are available, however, three different h values can be calculated from any set of experimental data.

Heat transfer coefficient based on Tad

This method of determining heat transfer coefficient was discussed in details in

chapter 6. The h value based on this method of analysis is a function only of geometry and flow condition. It is the only one of the four options whose value at a given location does not depend on the upstream heating pattern. Any investigation involving non-uniform heat release can only be analyzed using the T_{ad} .

Heat transfer coefficient based on T_{bulk}

With this method h is based on the mixed mean temperature. This type of analysis is most suited to conditions of uniformly powered PCBs, because there is no way to measure h_{bulk} experimentally without uniformly powering all the elements in the entire channel. The standard correlations show h_{bulk} to be a function of Reynolds number and fluid properties. Since in applications such as the present one, T_{bulk} remains constant, it follows that any variation in the h_{bulk} is entirely due either to Streamwise variation in film temperature near the surface or heat release in the module. To correlate the experimental data in this part of research, h was evaluated using the bulk mean temperature of the fluid.

7.7.2 HEAT TRANSFER WITH FULLY DEVELOPED FLOW (THERMAL BOUNDARY LAYER ANALYSIS)

In hydrodynamic fully developed channel flows the heat transfer coefficient of single powered element does not vary with streamwise position, hence there is no distinction between the local and average values.

In order to verify this a series of eight experiments was carried out powering one row at a time, while the remaining seven rows were switched off. For each test the flow

and powering conditions were kept constant. The board was scanned in each case with the IR scanner after the steady state condition had been reached. The average temperature rise of each powered row was found to be the same irrespective of its location on the PCB, hence confirming that each row was subjected to the same heat transfer coefficient, this indicates the existence of the fully developed boundary layer as illustrated in Figure 7.11 a to c.

7.7.3 FINITE ELEMENT SIMULATION OF THE THERMAL TEST BOARD

To construct a detailed FE model of the thermal test board exact knowledge of the internal structure of the PLCC package was required. Because of lack of information in manufacturer's data sheet, the top plastic moulding of a PLCC packages was filed away to reveal the chip, leadframe and the internal structure.

The general FE code ANSYS was used to construct a detailed, realistic three-dimensional model of the package and associated board. Because of their influence on the internal heat conduction path the model incorporated the leadframe and solder pads. Such a detailed model because of its size precluded the possibility of replicating the single package to form a complete PCB with eight modules. Figure 7.12 illustrates the construction of the FE model which consists of;

1) The printed circuit board.
2) PLCC package and leads.
3) The air gap between the package and PCB.
4) The solder pads on the PCB.

The PLCC module, the internal leadframe, solder pads and the PCB were constructed of three-dimensional isoparametric thermal brick elements (STIF 70), whilst the 3-

dimensional conducting bar element (STIF 33) was used to model the external leads.

1) ***The printed circuit board and the solder pads.***

The model of the PCB consisted of a single layer of epoxy with fine copper tracks for accurate modelling. The 23mm x 18mm x 1.6mm, section of the board associated with each package was modelled using a single layer of elements. It was assumed that, because of the size ratio between the copper tracks and the solder pads the heat conduction to the PCB was mainly significant at the solder joint and not along the copper tracks.

2) ***The PLCC package and leads.***

The PLCC package measuring 9mm x 9mm x 3.5mm was constructed of six layers of nodes and five layers of element, Figure 7.13. The top and bottom layers of elements represent the plastic molding encapsulant and a thin middle layer represents the leadframe and the chip elements. The two layers between the package and PCB represent the air layer. The power dissipation was then applied to the elements representing the chip in the centre of the model. The external leads, simulated by 3D conducting bars project from each node of the middle layer to the corresponding node on the solder pad on the board. A total of twenty leads were constructed to simulate the complete package.

7.7.4 BOUNDARY CONDITIONS FOR THE FE MODEL

The radiative power dissipation of each PLCC package was determined by calculation, using the Stefan-Boltzmann law, which was deducted from the total experimental power dissipation. The power input then corresponded to the internal heat generation

allocated to each of the chip elements in the model. For uniform power conditions full mixing of the heat transfer to the air stream was assumed, T_{bulk} was calculated using the energy balance equation. For each package and the associated board area uniform heat transfer coefficients was applied to all the exterior free surfaces of the model, except those facing into the package-board gap and the back of the board.

The under surface of the thermal test board was assumed to behave as a flat plate because, all the PLCC packages are mounted on the top surface of the board, and the hydrodynamic and thermal boundary layer starts developing from the leading edge of the thermal test board. Hence the heat transfer coefficient for the under surface of the board was calculated from the classical non-dimensional correlation of a turbulent flow over a flat plate:-

$$Nu_x = 0.0292\ Re_x^{0.8}\ Pr^{1/3} \tag{7.1}$$

where:-

Nu_x = Nusselt number
Re_x = Reynolds number
Pr = Prandtl number

From the definitions of Nusselt and Reynolds number, and since the properties of air are approximately constant over a wide range of pressure and temperature used in the experiments, the Prandtl number can be assumed constant at Pr= 0.707, equation 7.1 becomes:-

$$h = 0.0292\ \frac{K}{x}\left(\frac{Vx}{\nu}\right)^{0.8}\ 0.891 \tag{7.2}$$

The appropriate values of the heat transfer coefficient for the under surface of the board were calculated and incorporated in to FE model in form of a user file

(CVBT.UFL) for the velocities used. The natural convection effects were calculated and found to be negligible ie:($Gr/Re^2 << 1$) for the velocity range used.

The method of using the FE model to determine the heat transfer coefficient from the experimental data was similar, as described in (section 3.9.3) Chapter 3.

7.8 THE THERMAL CONDUCTIVITY OF THE PLASTIC PACKAGE

The ability of the chip, leadframe and the plastic encapsulant to conduct the heat from the chip to the ultimate sink is directly related to the thermal conductivity of the materials used. Molding compounds used for encapsulating chips in plastic packages are modified epoxy resins.

Epoxies are good adhesives, readily forming chemical bonds with the surfaces of the leadframe. However their thermal expansions coefficient is different from that of leadframe. To overcome this undesired effect, the moulding compounds are modified by addition of inert materials called fillers. The thermal conductivity of the encapsulant may be varied depending on the type and volume of the filler used. This information unfortunately is considered as commercially classified and is not published in the manufacturers data sheets.

7.8.1 DETERMINATION OF THE THERMAL CONDUCTIVITY OF ENCAPSULANT

For accurate predictions from the FE model, it was essential that thermal conductivity of the encapsulant be accurately known. To determine this two different methods were used;

1 The combination of FE and IR measured temperatures
2 Experiments.

1) ***Prediction of the K value using the IR and FEM***

Initially the thermal test board's row two was powered, 1 Watt/chip under forced convection at velocity of 4 m/s. After steady-state conditions had been reached, the board surface area corresponding to a similar area as the FE model was scanned both on the top and under surface with the IR scanner. Thermal images was produced in each case using the image processing program, whilst the SID was used to measure the V_{be} (base emitter voltage drop). The V_{be} voltage was readily converted to temperature using the calibration chart. Similarly the thermal image cursor probe was used to reveal the experimental surface temperature of the package and the associated board area on both side of the thermal test board, according to the nodal coordinates of the FE model.

These values of the surface temperature were applied to the appropriate nodes in the FE model using the temperature constraint (NT command), whilst removing all convection from the model. The heat generation rate of 1 Watt/volume of the element was also applied to the chip element in the model. With the present boundary condition (NT and internal heat generation), the only unknown quantity was the

thermal conductivity of the package encapsulant. By trial and error varying the plastic package thermal conductivity, the temperature of the chip in the FE model was matched to that of the SID . The required value of thermal conductivity to match the junction temperature (SID) in the FE model was 4.1 W/mK.

As a quick check with the plastic conductivity of 4.1 W/mK, the NT values in the model was replaced with convection to all the exterior surfaces apart from the ones already mentioned. The h value for the convective surfaces was obtained from the h characteristic curves (discussed latter). Figure 7.14 shows the comparison of the FE prediction with IR.

2) ***Experimental measurement of K value***

A PLCC package assembly was hand filed until the bottom plastic encapsulant, leadframe and the chip were removed. The remaining top plastic encapsulant then formed the test piece, which was incorporated into a especially designed and built conductivity test rig, as shown in Figure 7.15.

The test rig to measure the thermal conductivity of the plastic encapsulant, was constructed of polystyrene coated with a thin film of silicon rubber, to minimise the heat loss and avoid water leakage. In the cold channel, water was made to flow past the test piece (plastic encapsulant) at a constant rate at 20°C. On the hot side the water was heated via a 2 Ω resistor at a constant power dissipation of 18 watts, in a stationary insulated water tank to temperature of 100°C. To measure the steady-state temperature gradient across the plastic, two thermocouples were attached on either side of the test piece. Simultaneously a total of four thermometers was used to measure the

temperature of the free stream and hot water tank during the test.

Modelling the system as a plane wall with a moving fluid on one side and a stationary fluid at constant temperature, the heat transfer in the rig can be expressed in terms of the "overall rate equation"1

$$Q = -UA\ (T_H - T_C) \tag{7.3}$$

where:-
U = overall heat transfer coefficient. (W/m^2K)
1/UA = overall thermal resistance.(K/m)

Since for the rig's plane walls there are two resistances in series, the overall thermal resistance from equation 7.3 can be expressed as:-

$$\frac{1}{U} = \frac{1}{h} + \frac{\Delta x}{k} \tag{7.4}$$

Where $\Delta x/k$ is the resistance of polystyrene = 0.024/0.08

Assuming natural convection, (5 W/m^2K) of the surrounding air, the exposed sides of the rig yields (U = 2). Using this value of U all the losses through the rig walls were calculated and deduced from the total power dissipation. The conductivity of the plastic was then calculated from Fourier's law of conduction (see chapter 3), to be 3.97 W/mK. This value of conductivity is within 3% of the predicted value using the FE model.

7.8.2 EVALUATION OF THE PACKAGE THERMAL RESISTANCE USING FE AND EXPERIMENT

The method of analyzing thermal performance of an electronic package using the concept of thermal resistance was described in Chapters 3 and 4. This method was used to validate the two K values obtained from experiment and combined FE and IR for the PLCC package encapsulant.

The junction to ambient (${}_JR_A$) thermal resistance recommended by Texas Instrument for a twenty pin PLCC is in the order of 103 °C/W, as shown in Figure 7.1b.

A series of tests involved uniformly powering the thermal test board under forced convection conditions. Steady-state values of junction (SID) and surface (IR) temperatures were recorded and used to evaluate the internal and external thermal resistances of the PLCC package. Similarly FE runs were carried out corresponding to the test conditions, from which the internal and external thermal resistances were also evaluated as shown in Table 7.1.

THERMAL RESISTANCE	${}_JR_A$	${}_JR_C$	${}_CR_A$
TEXAS INST.	103.6	37.1	66.5
EXPERIMENT	55.0	17.2	37.5
ANSYS	56.75	18.3	38.45

Table 7.1 comparison of thermal resistance package mounted on PCB

Analysis of Table 7.1 initially indicates that the ANSYS and experimental values of thermal resistance is about half the values reported by Texas Instruments. However, after a thorough analysis and series of discussions with Texas Instrument it was revealed that the reported values of thermal resistance by them is not for the conditions tested (package mounted on PCB). To validate the PLCC's encapsulant thermal conductivity numerically (FEM), using the concept of thermal resistance, new FE runs and test arrangement was necessary.

A new test arrangement involved suspension of a single PLCC package with out PCB in natural convection as shown in Figure 7.16.

The electrical connections to each lead was made by very fine wires to minimise if not totally eliminate conduction through the leads. which served to power the package.

In series of FE runs the PCB elements were selected and deleted from the model simulating the test conditions. Heat transfer coefficient for the FE model, (package in natural convection) was calculated from equations 3.17 and 4.6 (Chapters 3 and 4). The junction and surface temperatures were recorded and used to evaluate the thermal resistance. The values of thermal resistances for a single package suspended in air is illustrated in Table 7.2.

THERMAL RESISTANCE	${}_JR_A$	${}_JR_C$	${}_CR_A$
TEXAS INST.	103.6	37.1	66.5
EXPERIMENT	106.6	30.21	76.39
ANSYS	109.6	32.32	78.27

Table 7.2 comparison of single package thermal resistance

The thermal resistance values using the above method are on average with in 5% of the values recommended by Texas Instrument. However the Texas Instrument thermal resistance data as shown in Figure 7.1b were found to be very ambiguous. Care should be taken when defining the thermal resistance as it can be seen the effect of removing the board is to markedly increase the junction and hence the case temperature resulting in higher thermal resistances. This analysis is in line with the analysis presented in chapter 5 when a single DIP was analyzed with and without PCB.

7.9 HEAT TRANSFER CORRELATION OF THE THERMAL TEST BOARD

A series of experiments was carried out at four different power dissipations (0.5 - 2 W/chip) and air velocities ranging from 1.6 - 8 m/s. In each case the thermal test board was scanned with the IR scanner and a thermal image was produced using the image processing program.

Figures 7.17a and b show typical thermal images corresponding to a range of velocities obtained during the test. Similarly the temperature distribution along the thermal test board from the above thermal images are illustrated in Figures 7.18a-d.

An equation which correlates the heat transfer coefficient at any streamwise location was sought in the form:-

$$h_x = C \frac{v^{0.8}}{x^m} \qquad (7.5)$$

where:-
C and m = Unknown empirical correlation constants.
where
x = The distance from the leading edge of the board (m).
h_x = Heat transfer coefficient at distance x (W/m^2K).
V = Velocity, value of velocity 0.8 index is consistent with established correlation of turbulent boundary layer flow.

The values of C and m were obtained by plotting log(h)-0.8log(V) against log(x) for all the experimental data.

The method of using the FE model to determine the heat transfer coefficient from the experimental data was similar to that described in chapter 3. For a fixed value of power dissipation and zero ambient temperature, the FE model was run with a series of different heat transfer coefficients. A plot of heat transfer coefficient against the temperature of a particular point on the package surface (maximum surface temperature) for each of the experimental power dissipations is illustrated in Figure 7.19. This figure in conjunction with the experimental temperature difference was then used to extract the h values at any streamwise location.

The values of c and m (equation 5.8), were obtained by plotting log(h)-0.8 log(V) against log(x) for all the experimental data Figure 7.20. A first order regression fit (least-squares straight line) yielded the required values of C=13.95 and m=0.171 in equation 5.8 giving:-

$$h_x = 13.95 \frac{v^{0.8}}{x^{0.17}} \qquad (7.6)$$

It is also an accepted practice to express the heat transfer correlation in non-dimensional form by plotting the Nu (Nusselt number) against the Re (Reynolds number) as illustrated in Figure 7.21. At test conditions the Prandtl number for air has an approximately constant value of 0.707. This yielded the following correlation:-

$$Nu_x = 0.0668\ Re_x^{0.82}\ Pr^{1/3} \qquad (7.7)$$

Analysis of the above two correlations revealed they correlated the experimental data within 7 - 10 %.

For ease of programming, the correlation given in equation 7.6 was incorporated in an ANSYS user file (BOND.UFL). The values of air velocity V, power dissipation and distance x along the PCB x were automatically indexed by the program to simulate all the experimental tests. A comparison of experimental and FE predicted surface temperatures are shown in Figure 7.22 a and b. The agreement was good over the entire range of the tests. Apart from the case of high power dissipation and low velocity the surface temperatures of the PLCC packages were predicted with in 2 -3 degrees.

As already mentioned, because of the scarcity of performance data in literature, it was not possible to carry out a comparison of the correlation derived by the author with that of the other researchers. However the correlation above was compared with the

available flat plate correlation equation 7.1.

Making the appropriate substitutions in this equation yields;

$$h_x = 4.75\frac{V^{0.8}}{X^{0.2}} \qquad (7.8)$$

A comparison of the correlations in equations (7.6) and (7.8)
shows that the h values from the test board are some 2.9 greater than for a flat plate. The higher values are a consequence of the interrupted nature of the flow over the modules on the test board.

7.10 CONCLUSIONS

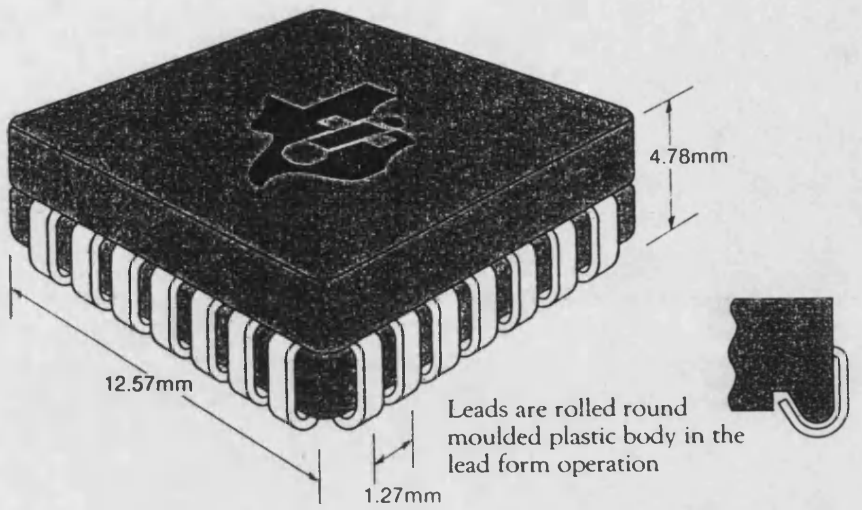
The major objectives of this part of the research were achieved. A thermal test board was designed and manufactured incorporating the state of the art surface mount packages PLCC (SN72501FN). A test rig was designed and built incorporating the infra-red techniques as a method of surface temperature measurements. The use of finite element in conjunction with infra-red image was found to be effective and superior tool compared to other numerical methods. The thermal conductivity of the plastic encapsulant of PLCC was deduced by combining IR images and FE predictions. Such thermal conductivity data is not available in the literature. The thermal resistances of 20 pin PLCC was investigated, and the effect of PCB on thermal resistance was analyzed.

The forced convection cooling of printed circuit boards with an array of surface mounted components, was also investigated, with a particular emphasis on measurement and prediction of heat transfer coefficient. The research reported here represents the first published correlation known to the author for heat transfer coefficients on an array of surface mounted devices mounted on a printed circuit board.

The finite element model revealed provided details of the temperature distributions within the package, solder pads and the board. The use of such a realistic model eliminated the need for those simplifying assumption which normally affects the accuracy of the purely analytic treatments.

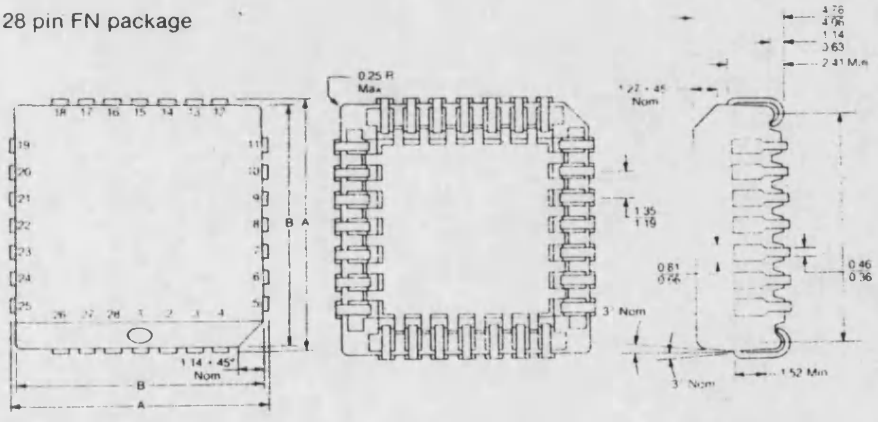
The use of a temperature sensitive parameter (SID) and infra-red imaging system made it possible to establish the thermal resistance of the PLCC package. Thermal resistances calculated in this way, and those from the FE model were found to be in line with those in the manufacturer's specification.

28-pin plastic leaded chip carrier



NO OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9.35	10.03	8.89	9.04	8.08	8.38
28	11.89	12.57	11.43	11.58	10.62	10.92
44	16.97	17.65	16.51	16.66	15.70	16.00
52	19.51	20.19	19.05	19.20	18.24	18.54
68	24.59	25.27	24.13	24.28	23.32	23.62

28 pin FN package



18 pin FP package

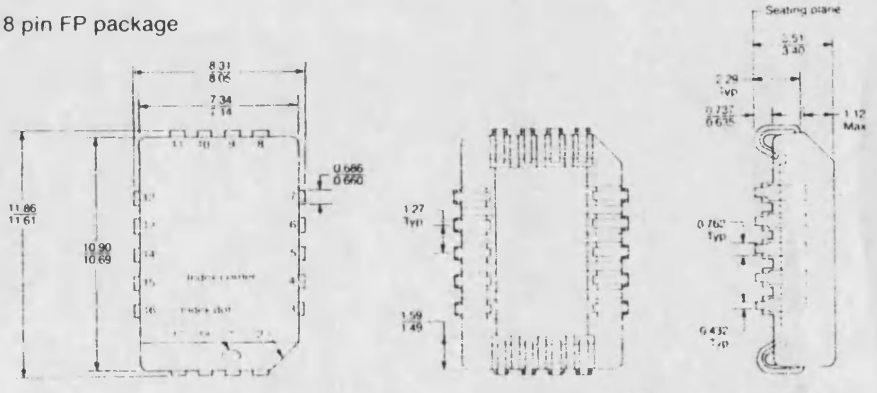


FIGURE 7.1a - SURFACE MOUNT 20 PIN PLCC PACKAGE

Plastic leaded chip carrier thermal characteristic

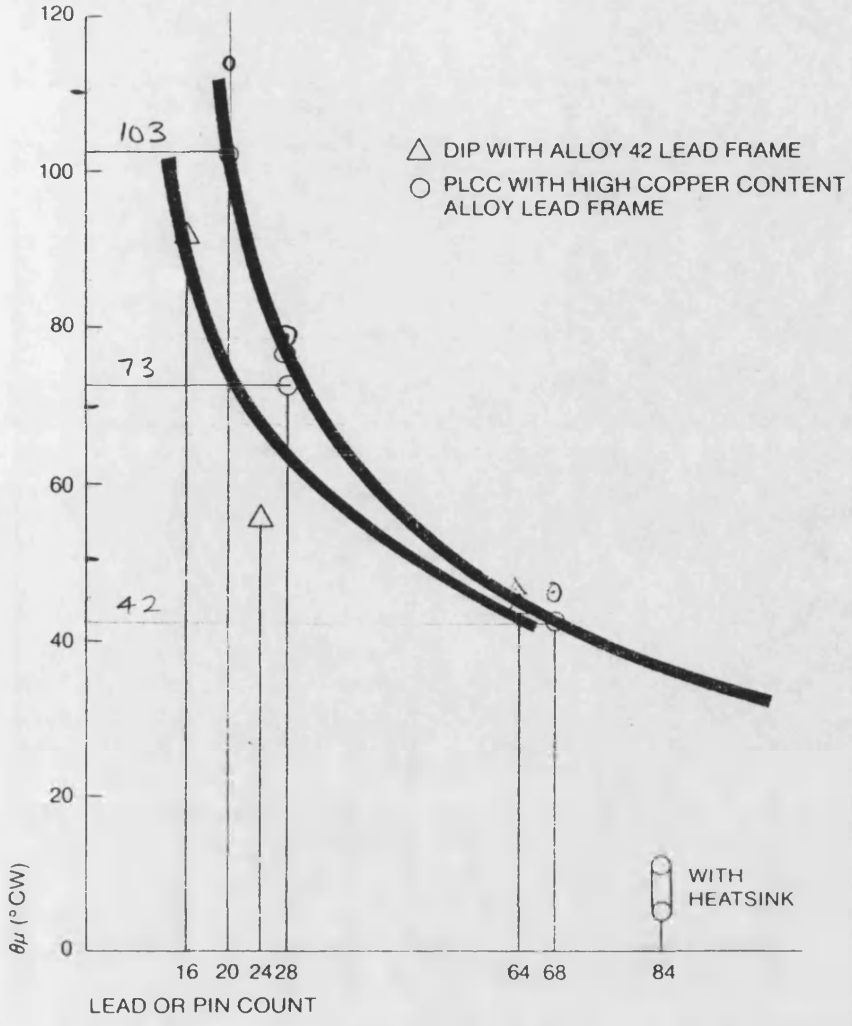


FIGURE 7.1b - TEXAS INSTRUMENT RECOMMENDED THERMAL CONDUCTIVITY

Pin Count	Package Designation	θJA (°C/W)	θJC (°C/W)
20 PLCC	FN	113.6	37.1
20 DIP	N	112.1	40.0
28 PLCC	FN	76.8	32.2
28 DIP	N	74.8	34.5
44 PLCC	FN	68.0	20.3
40 DIP	N	52.8	11.6
68 PLCC	FN	45.7	11.4
64 DIP	N	45.4	11.7

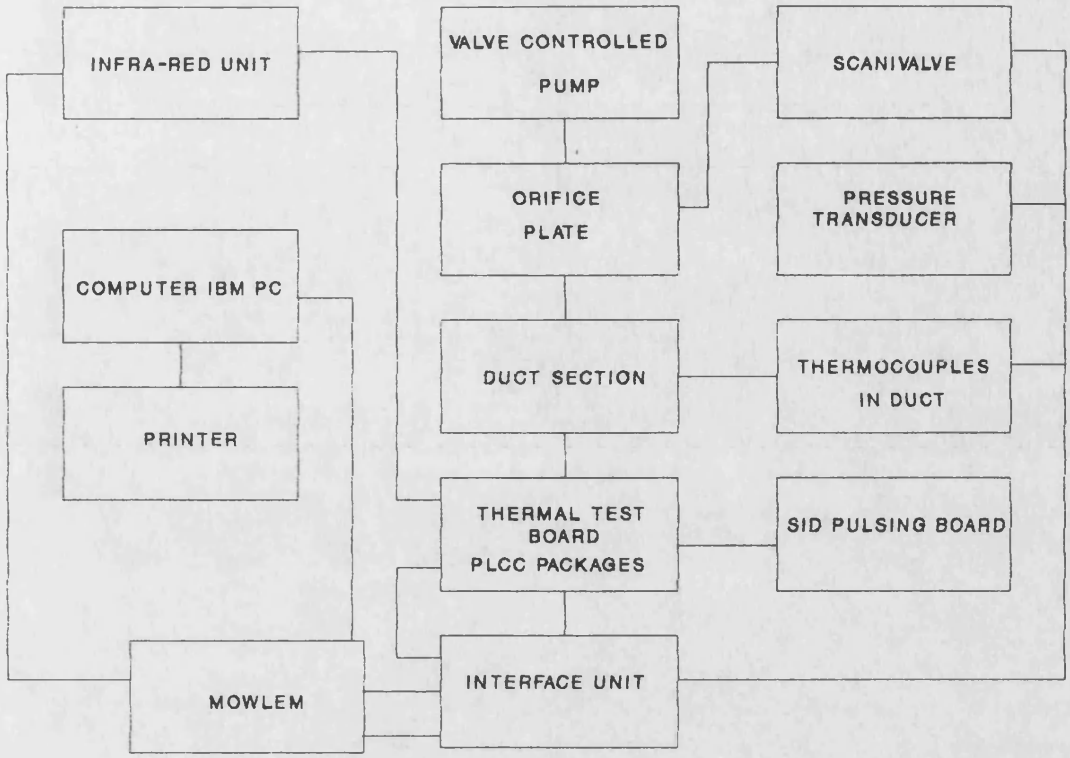


FIGURE 7.2a - TEST RIG ASSEMBLY BLOCK DIAGRAM

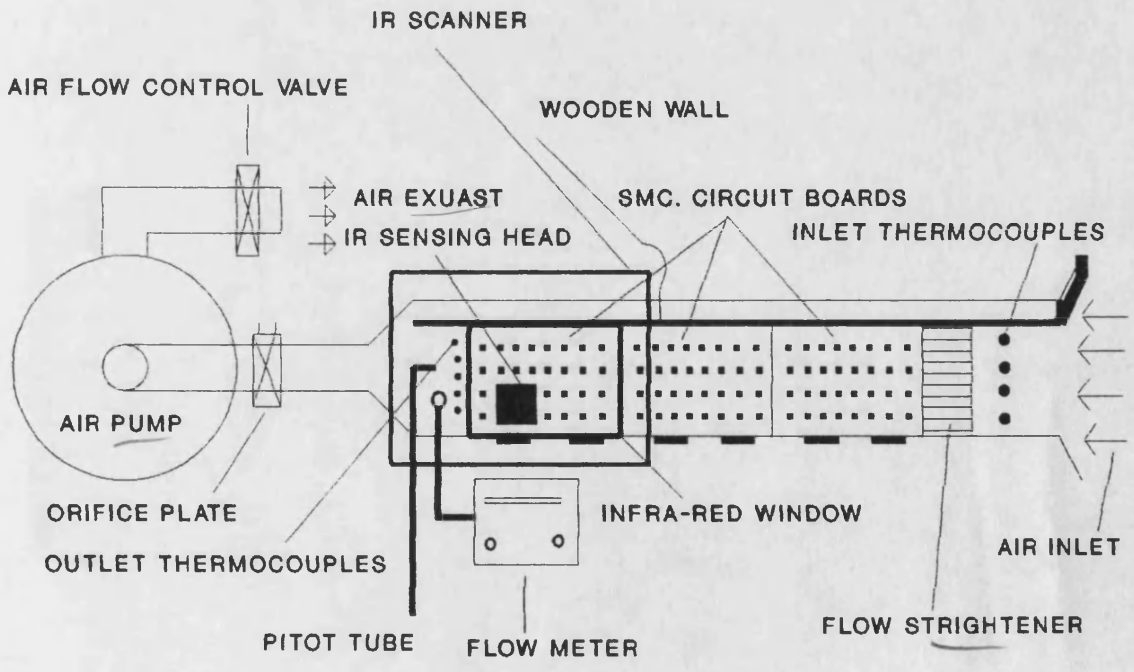


FIGURE 7.2b - GENERAL ASSEMBLY OF THE TEST RIG

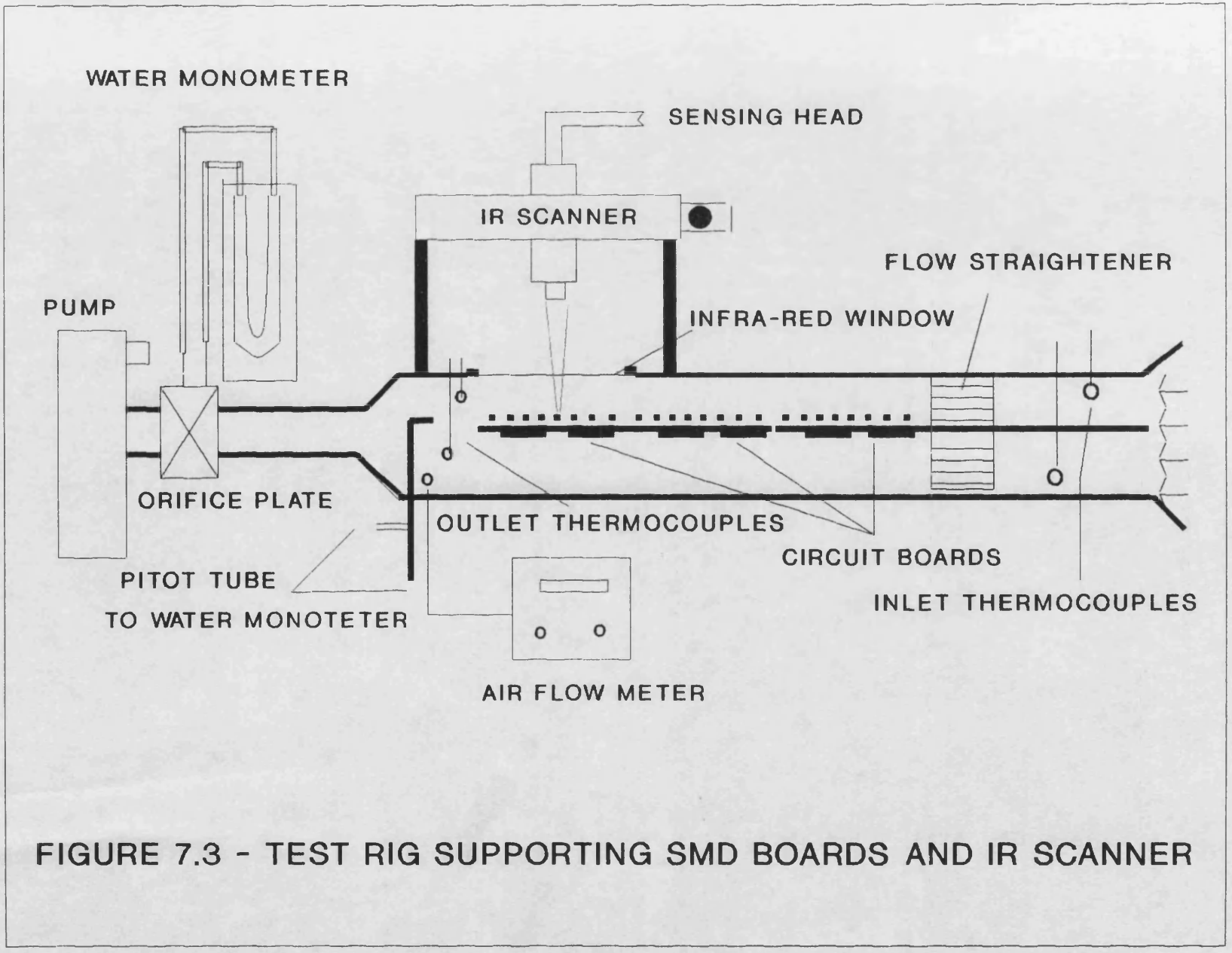


FIGURE 7.3 - TEST RIG SUPPORTING SMD BOARDS AND IR SCANNER

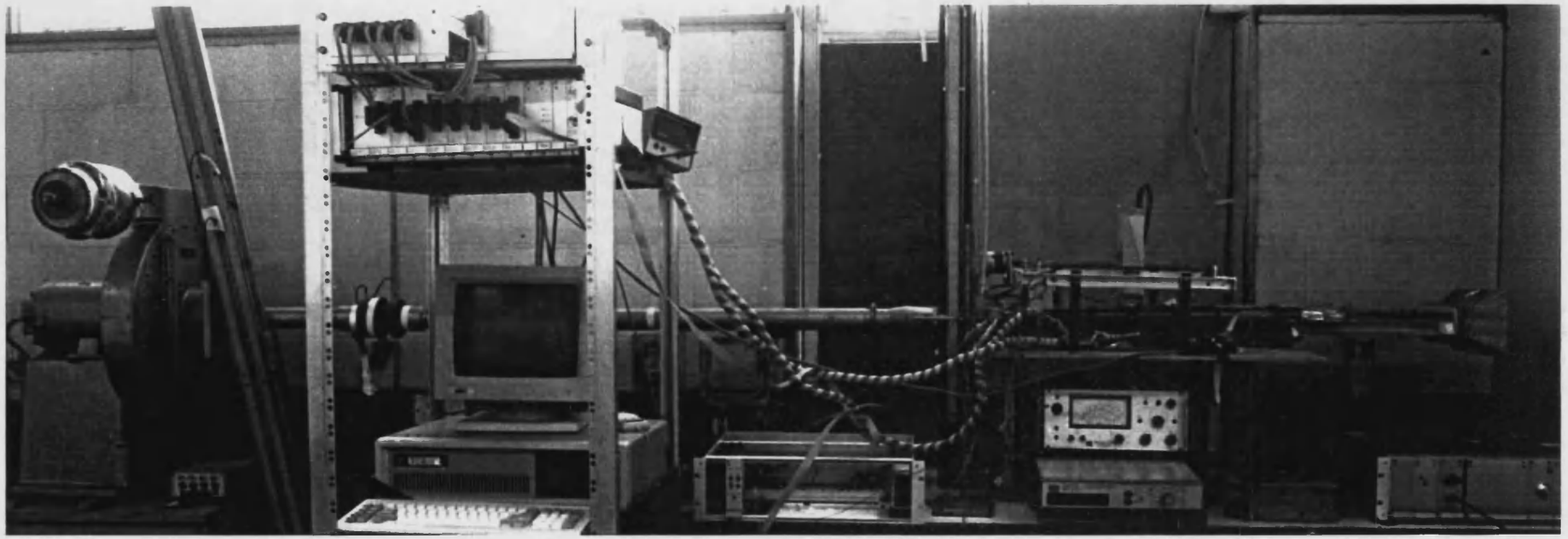


FIGURE 7.4 - PHOTO OF RIG ASSEMBLY

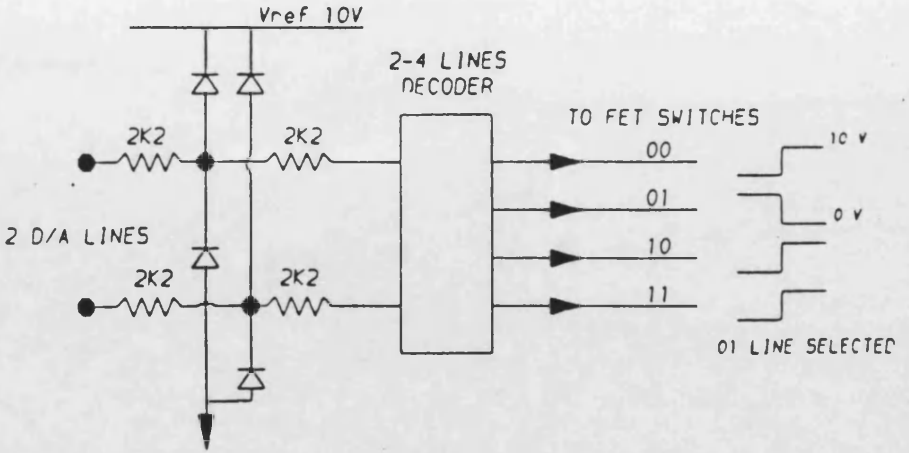


FIGURE 7.5b - CONTROL SELECT LINES WIRING DIAGRAM

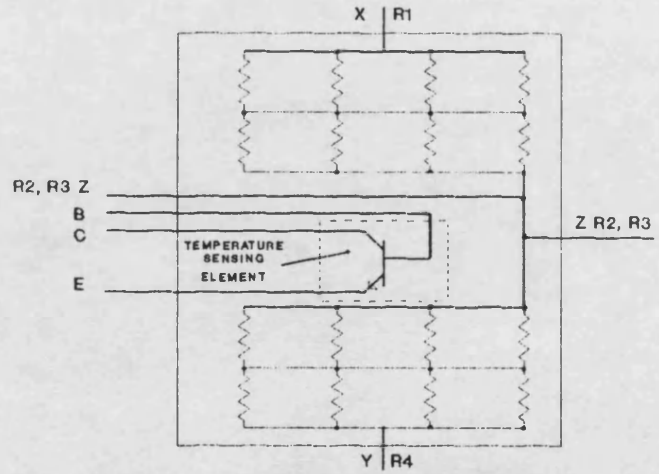


FIGURE 7.6 - INTERNAL CONSTRUCTION OF PLCC PACKAGE

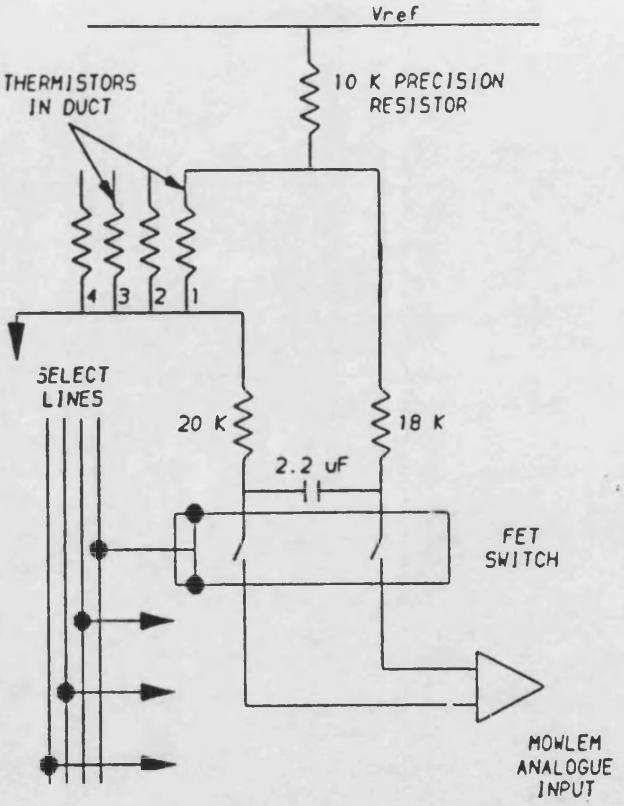


FIGURE 7.5a - SIGNAL MULTIPLEXING FOR ONE THERMISTOR

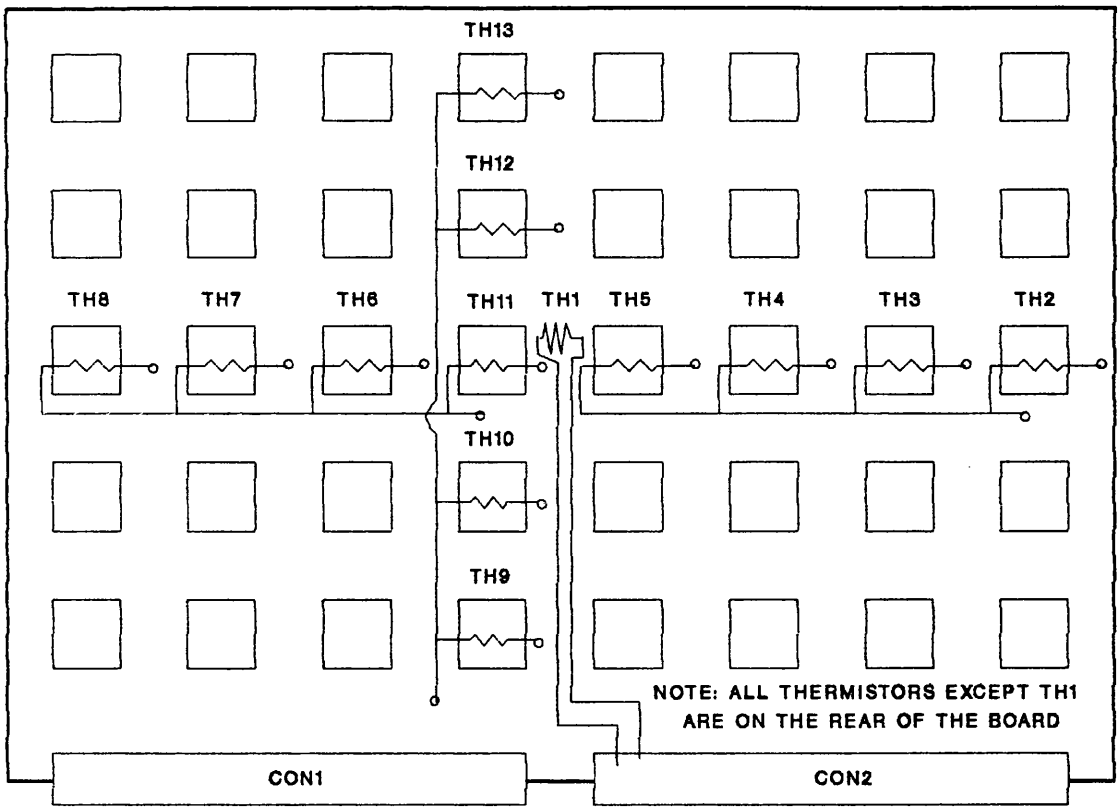


FIGURE 7.7a - COPPER TRACKS FOR THERMISTORS

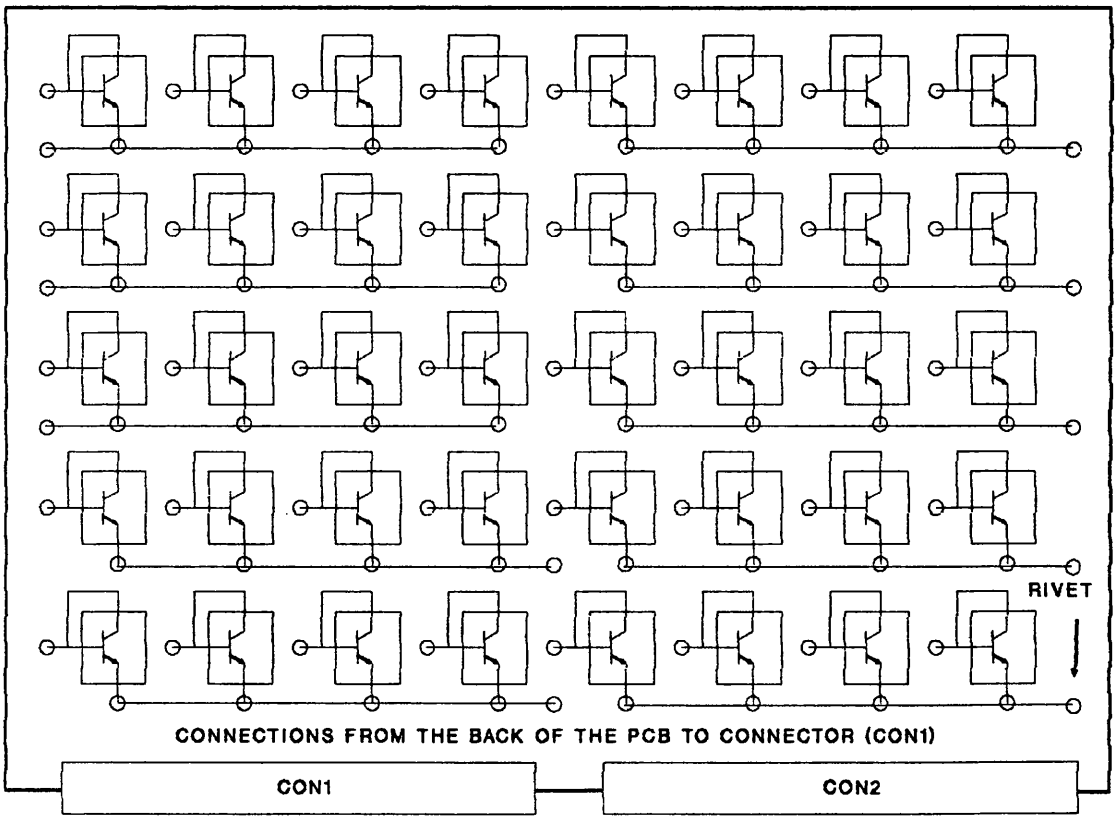


FIGURE 7.7b - COPPER TRACKS FOR TRANSISTOR BASE EMITTER

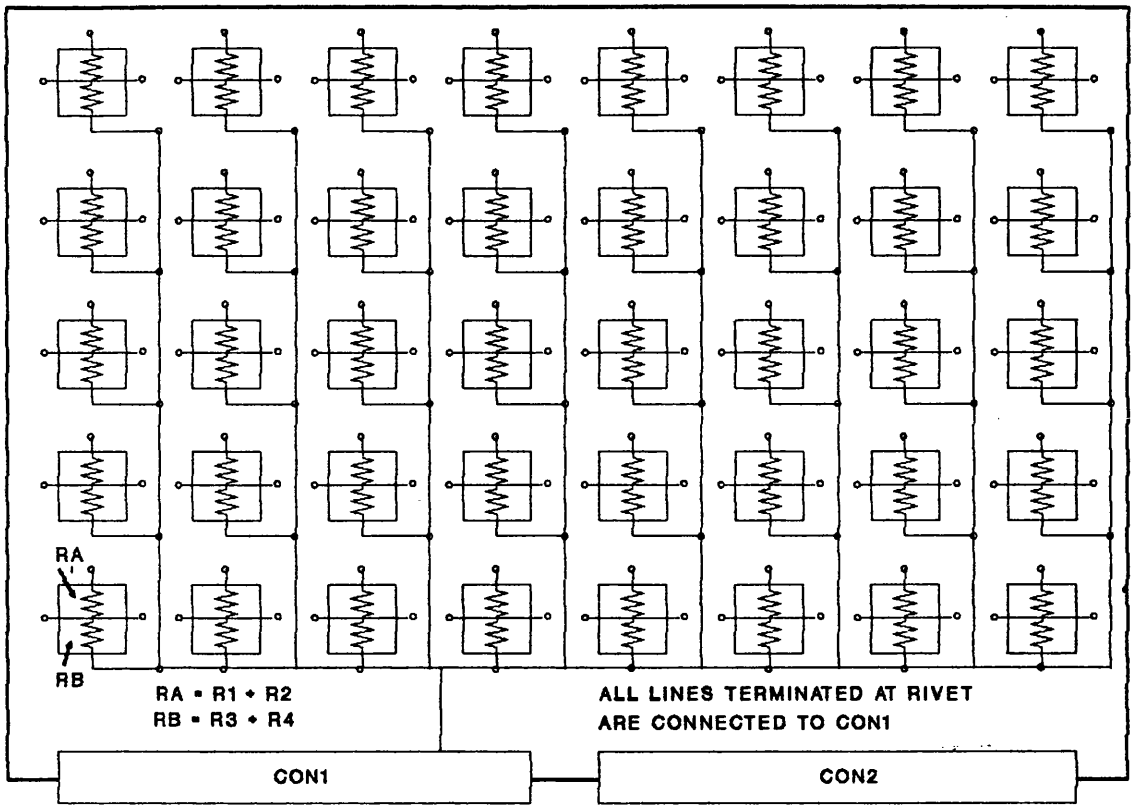


FIGURE 7.7c - RESISTANCE NETWORK COPPER TRACK LAYOUT

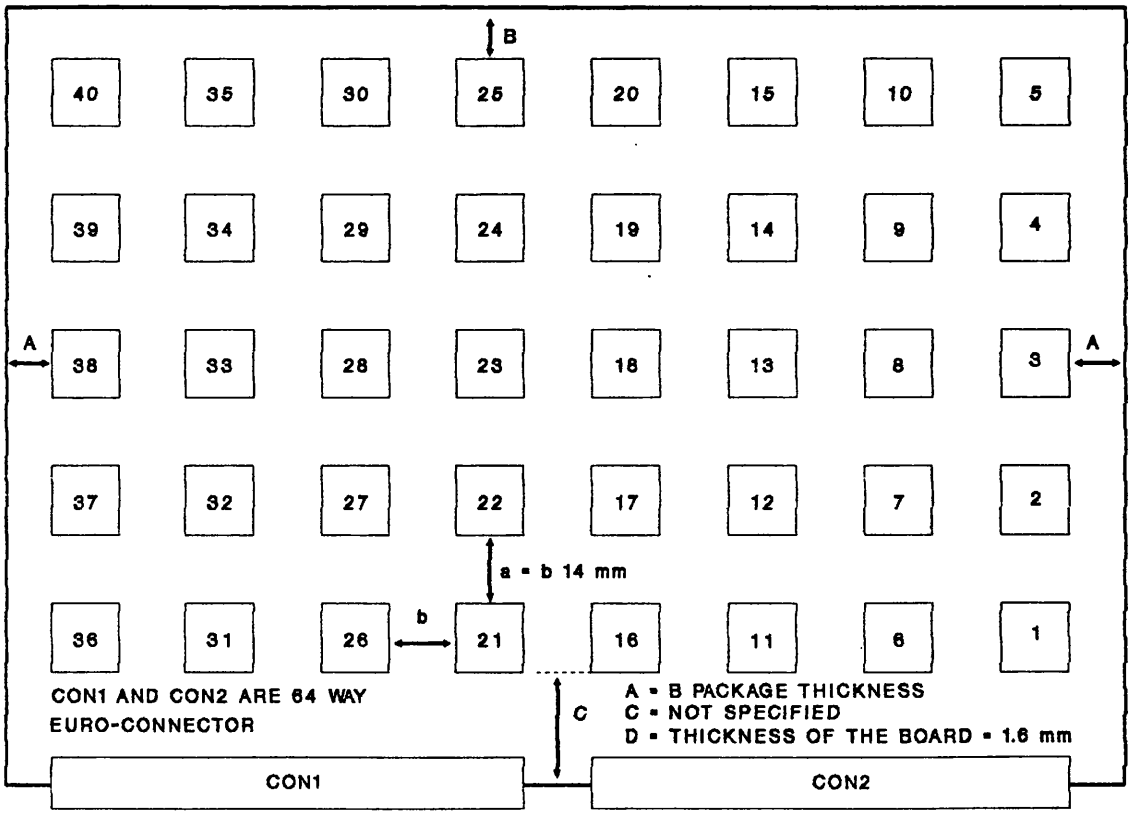
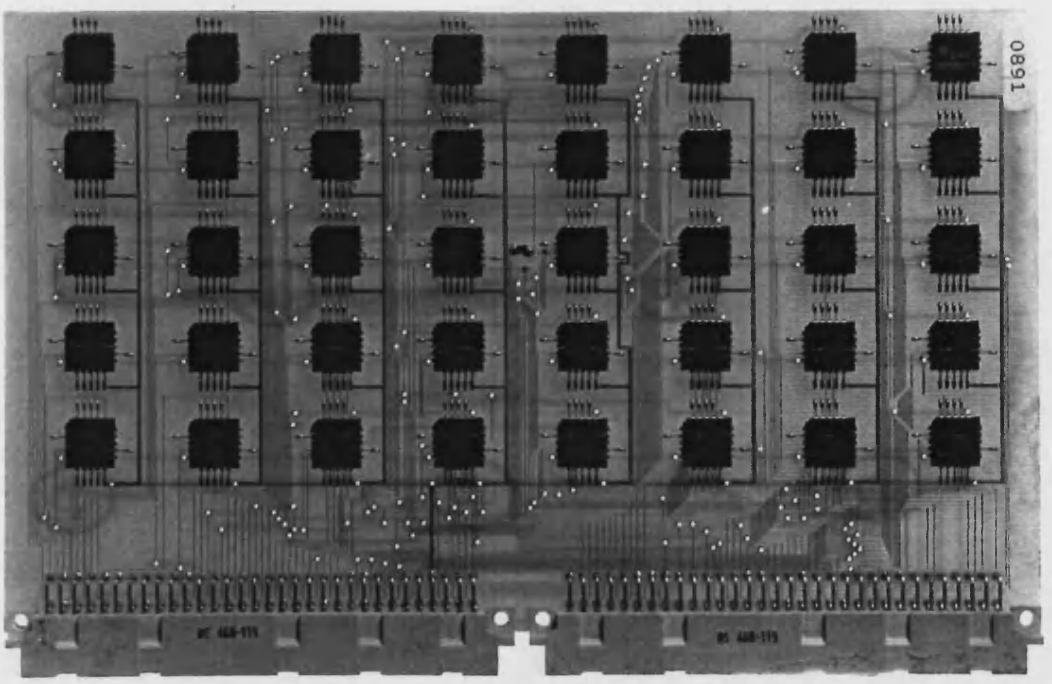


FIGURE 7.8 - THERMAL TEST BOARD (DEVICE LAYOUT)

TOP SURFACE



UNDER SURFACE

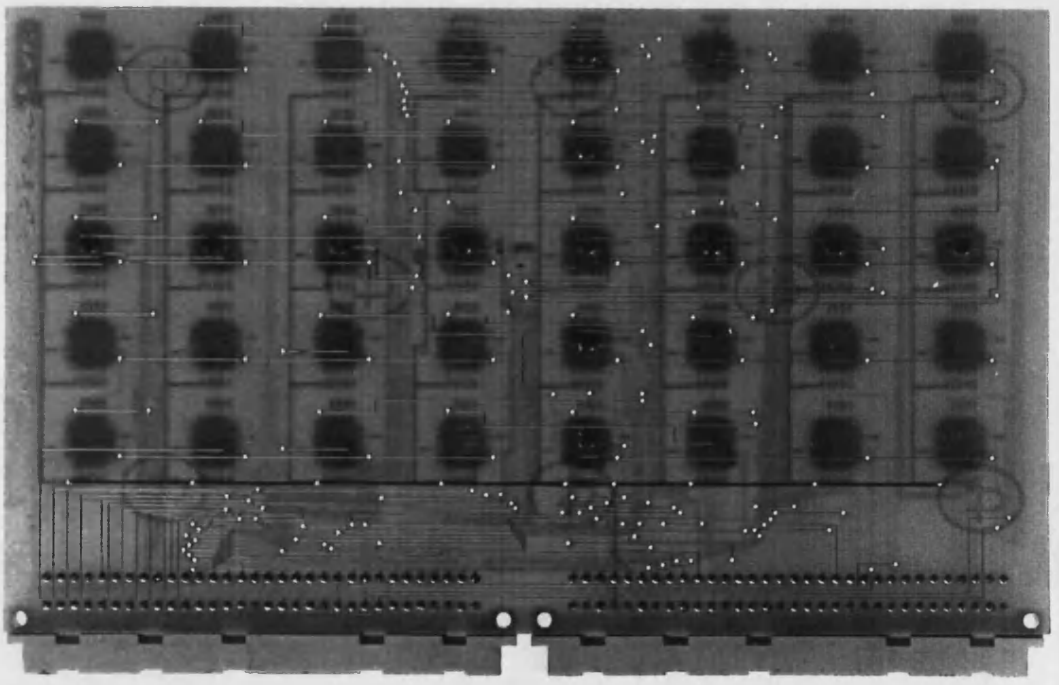


FIGURE 7.9 - PHOTO OF TEST BOARD

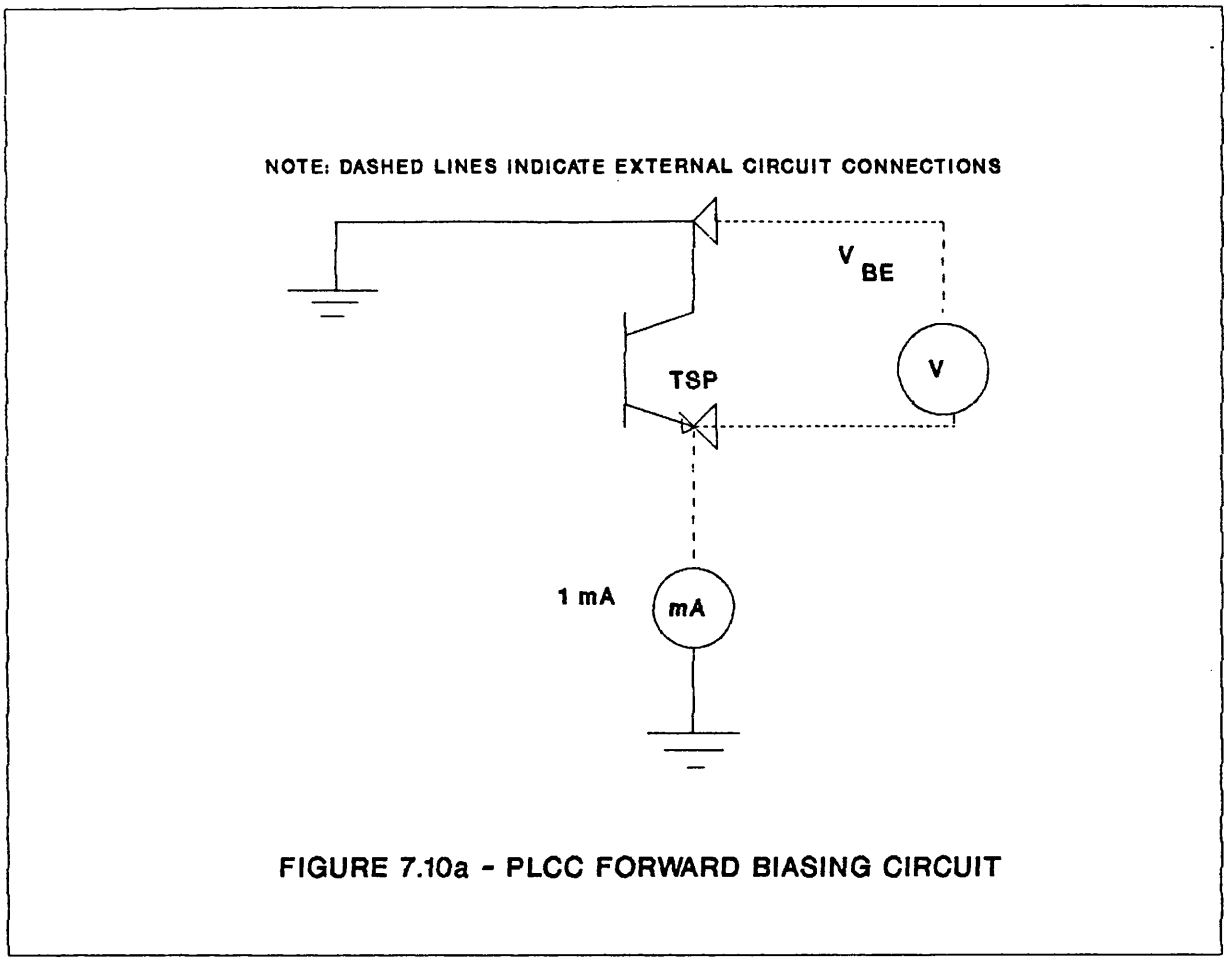
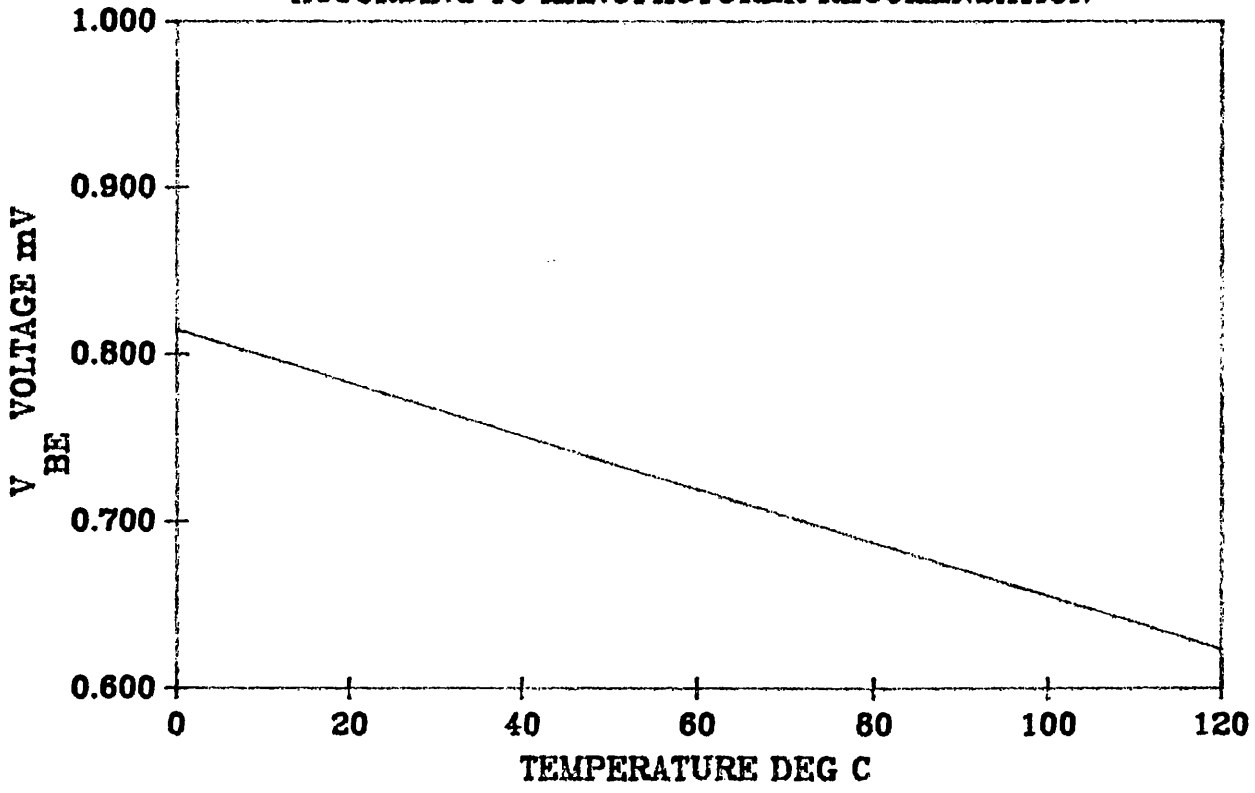


FIGURE 7.10a - PLCC FORWARD BIASING CIRCUIT

FIGURE 7.10b
CALIBRATION OF A PLCC PACKAGE (SN 72501 FN)
ACCORDING TO MANUFACTURER RECOMENDATION



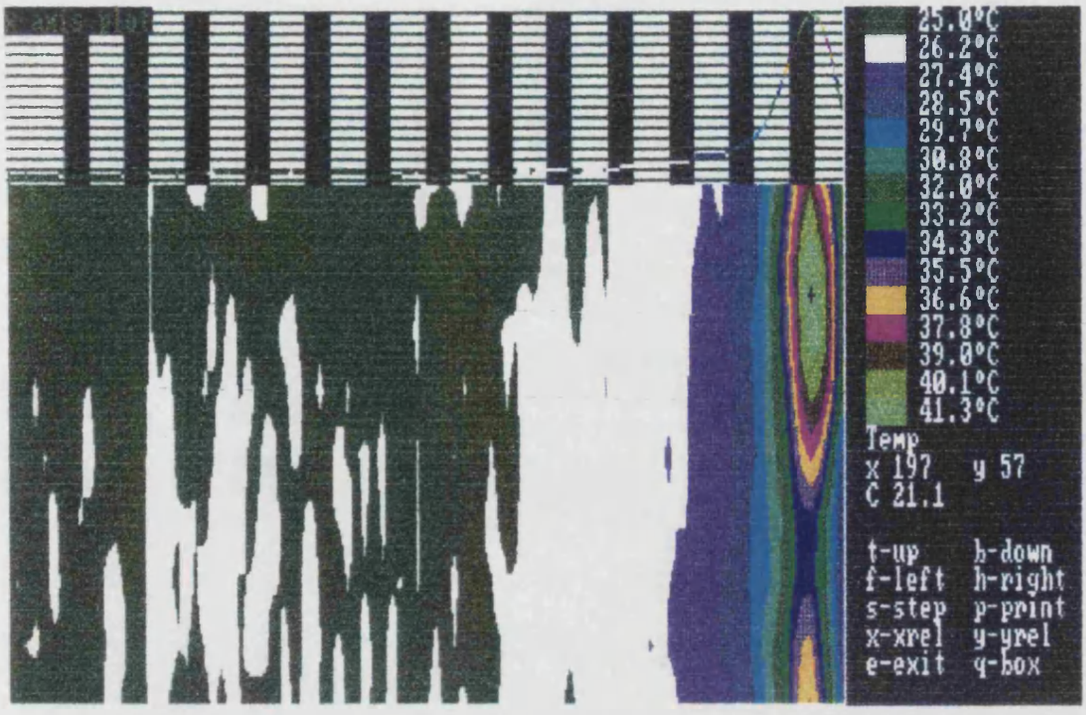


FIGURE 7.11a - THERMAL IMAGE OF ROW 1 POWERED
(BOUNDARY LAYER INVESTIGATION)

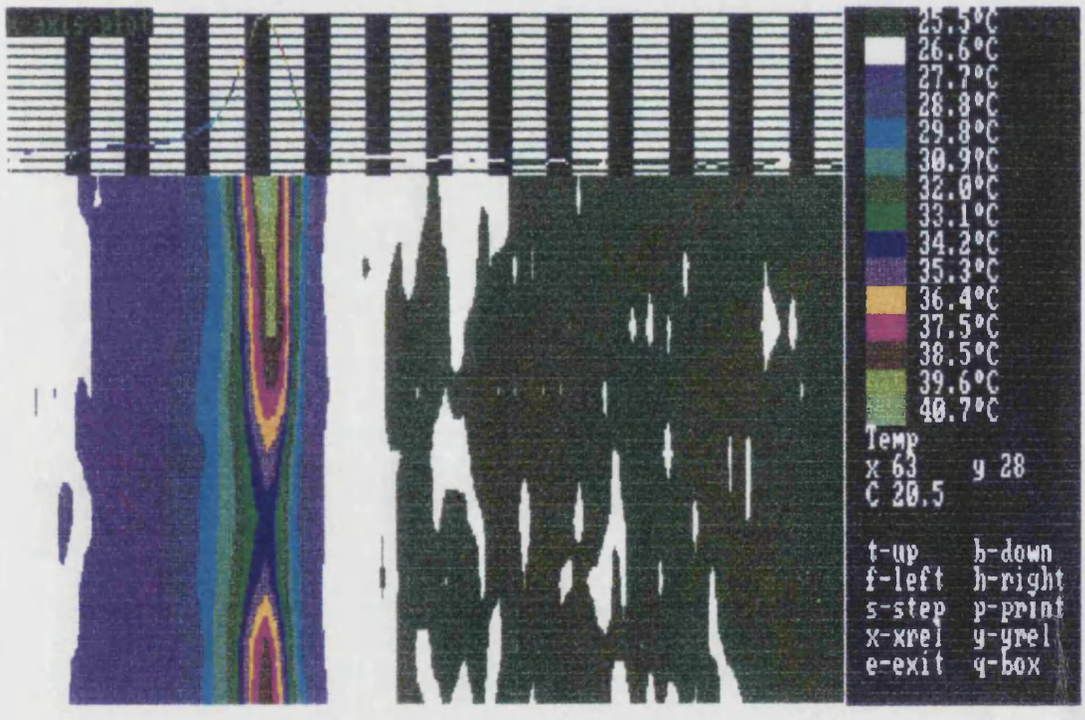


FIGURE 7.11b - THERMAL IMAGE OF ROW 6 POWERED
(BOUNDARY LAYER INVESTIGATION)

FIGURE 7.11c
THERMAL BOUNDARY LAYER INVESTIGATION

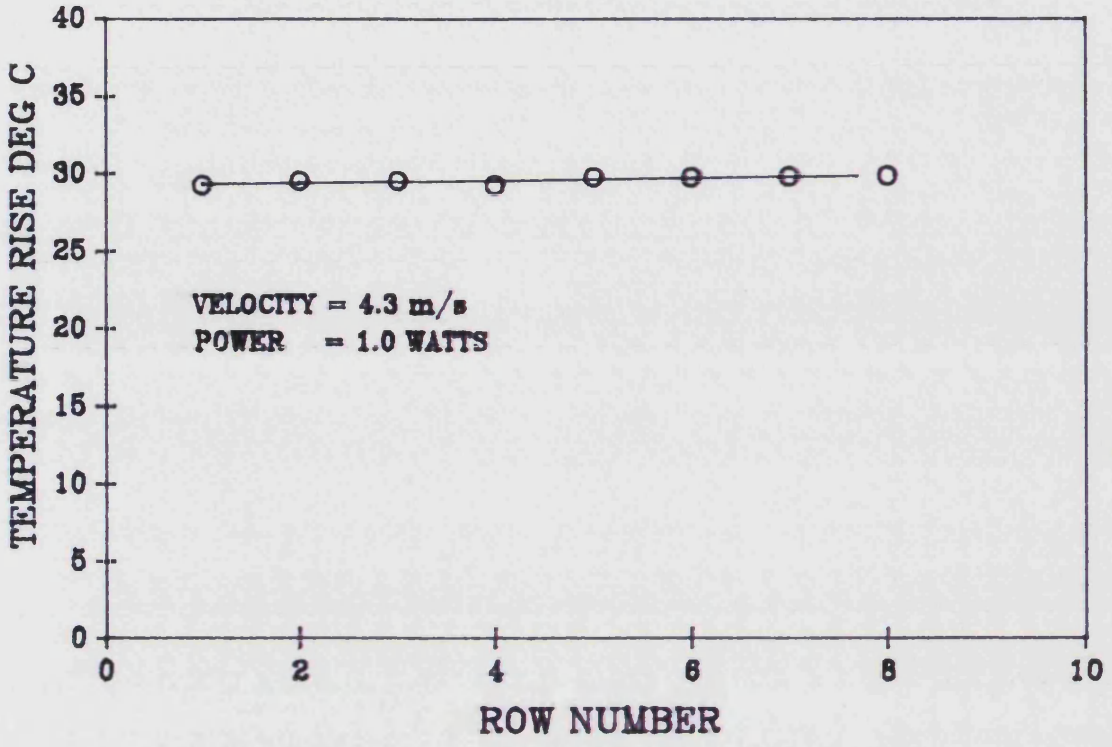


FIGURE 7.12 - CONSTRUCTION OF SINGLE FE MODEL

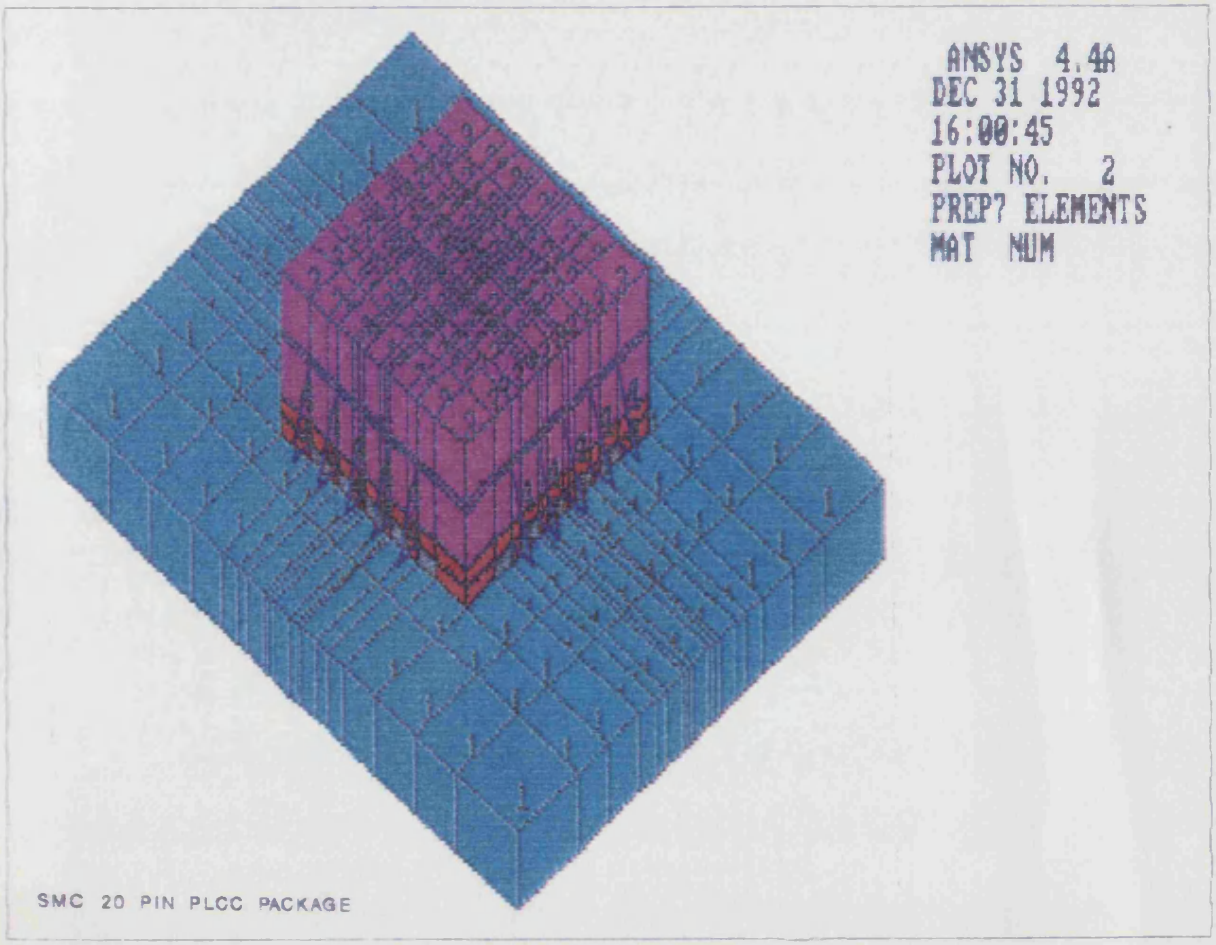


FIGURE 7.13 - CONSTRUCTION OF INTERNAL LEAD-FRAME CHIP AND SOLDER PADS

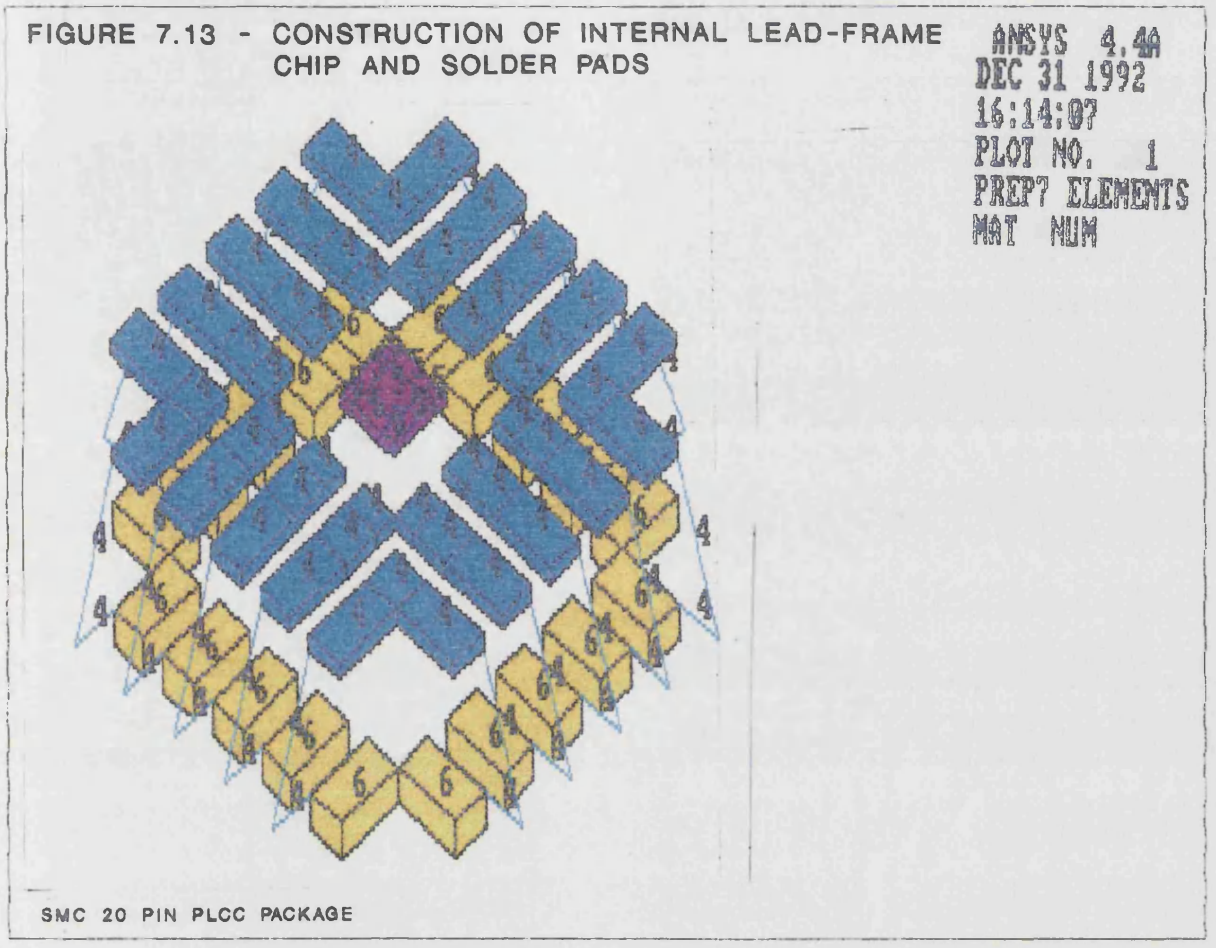
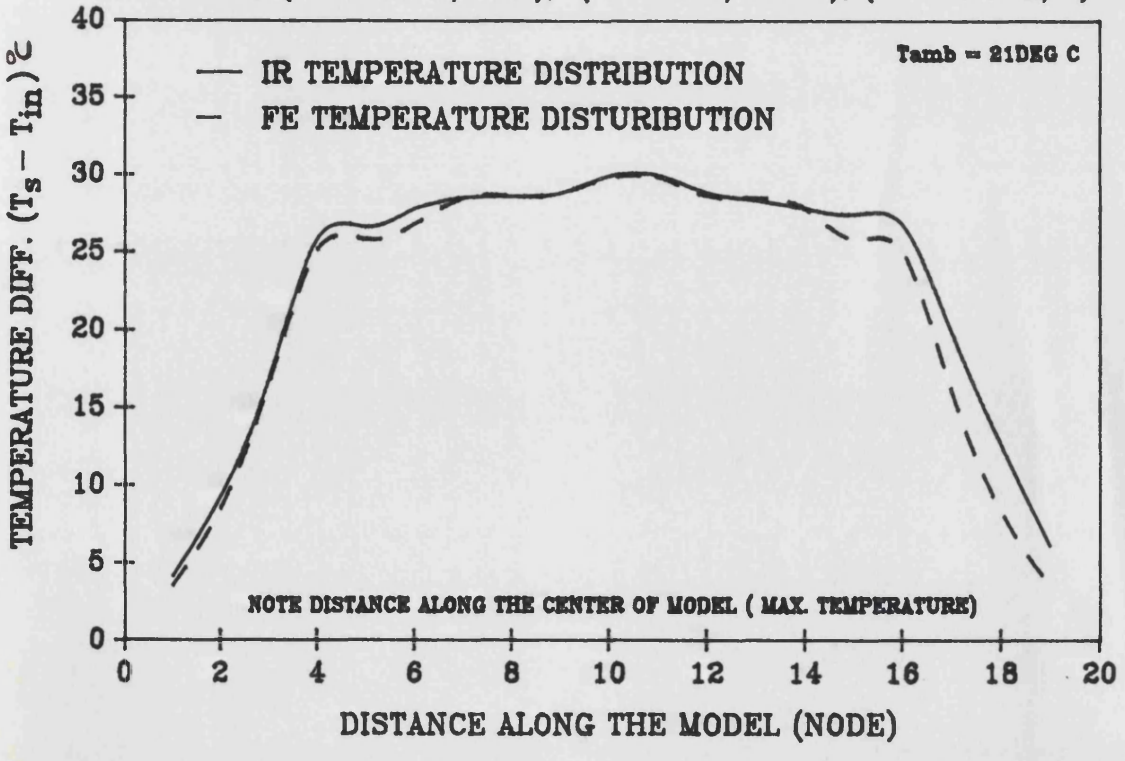


FIGURE 7.14

COMPARISON OF IR AND FE TEMPERATURE DISTRIBUTION

h IN PLACE (K = 4.1 W/mK), (W = 1 W/CHIP), (V = 4.3 m/s)



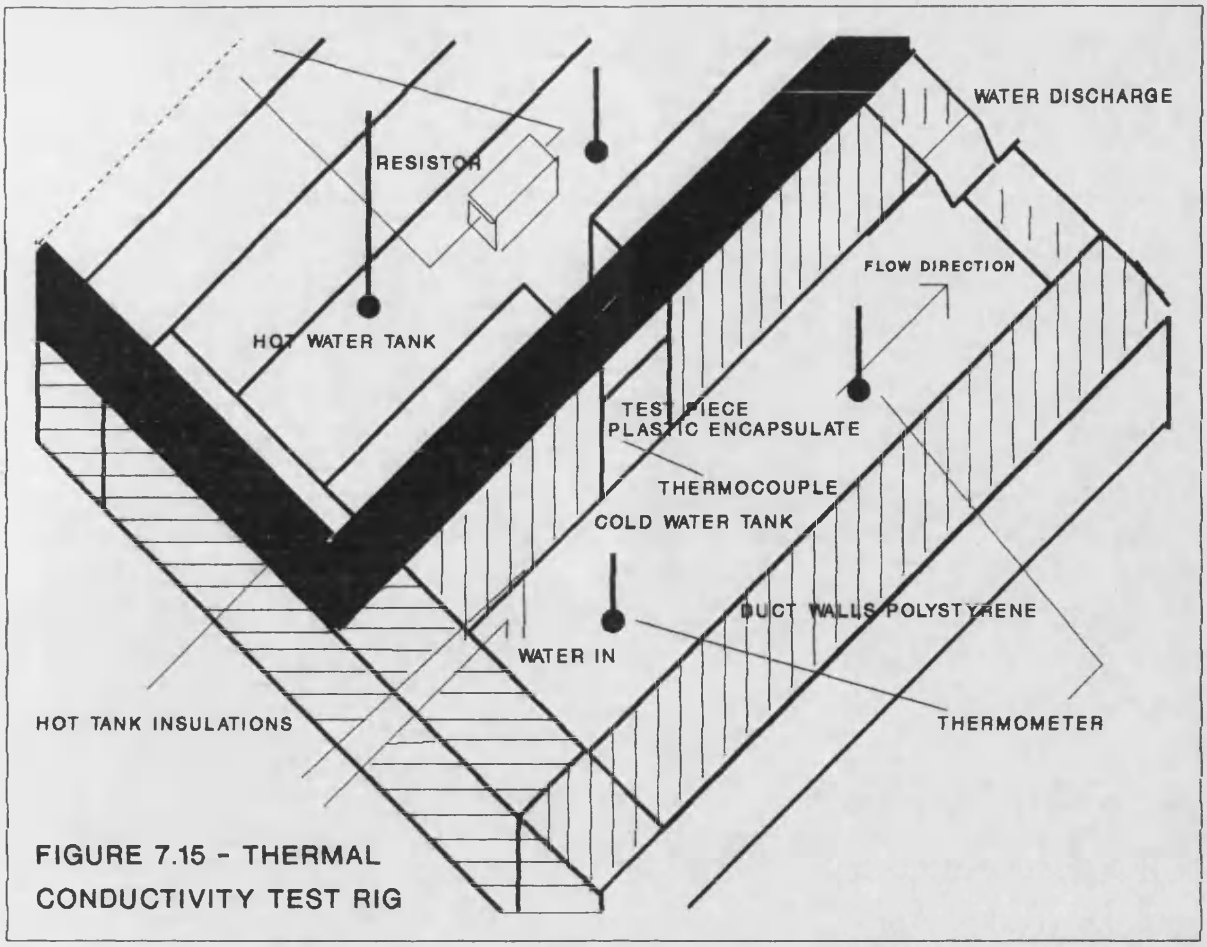
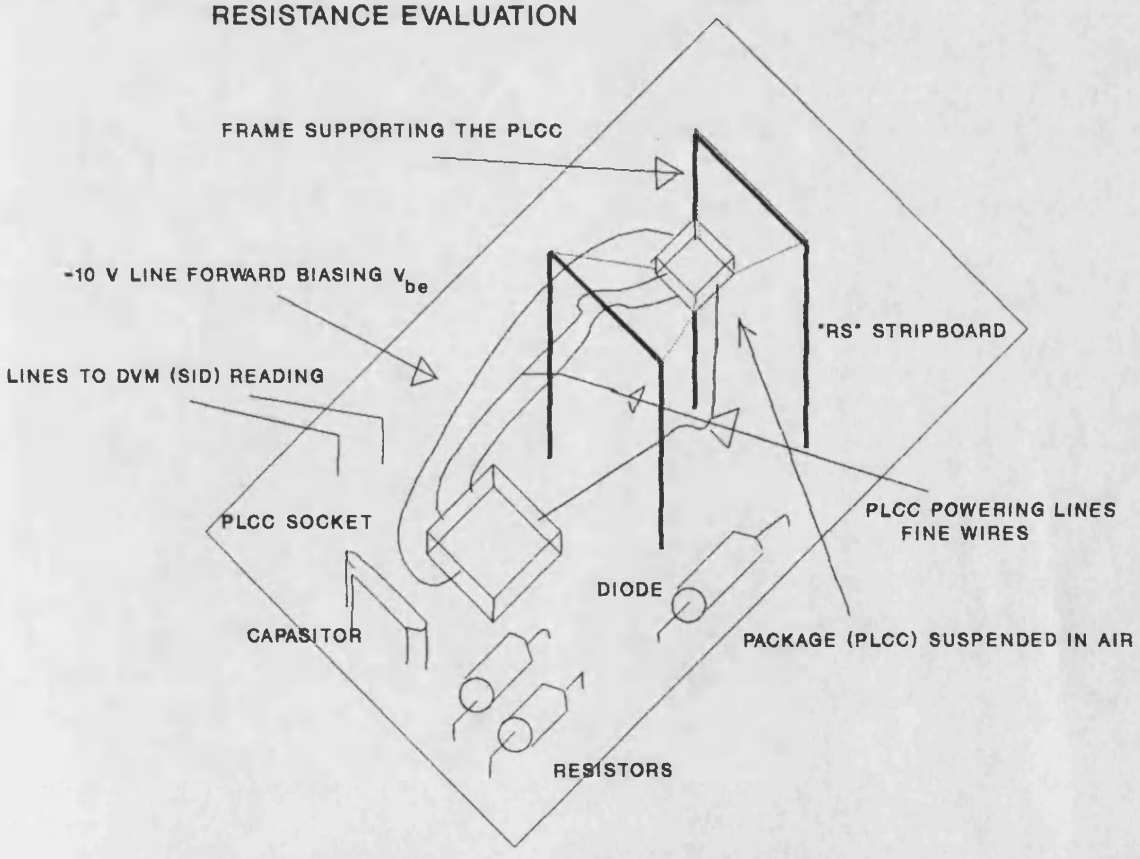


FIGURE 7.15 - THERMAL CONDUCTIVITY TEST RIG

FIGURE 7.16 - SINGLE PACKAGE TEST RIG THERMAL RESISTANCE EVALUATION



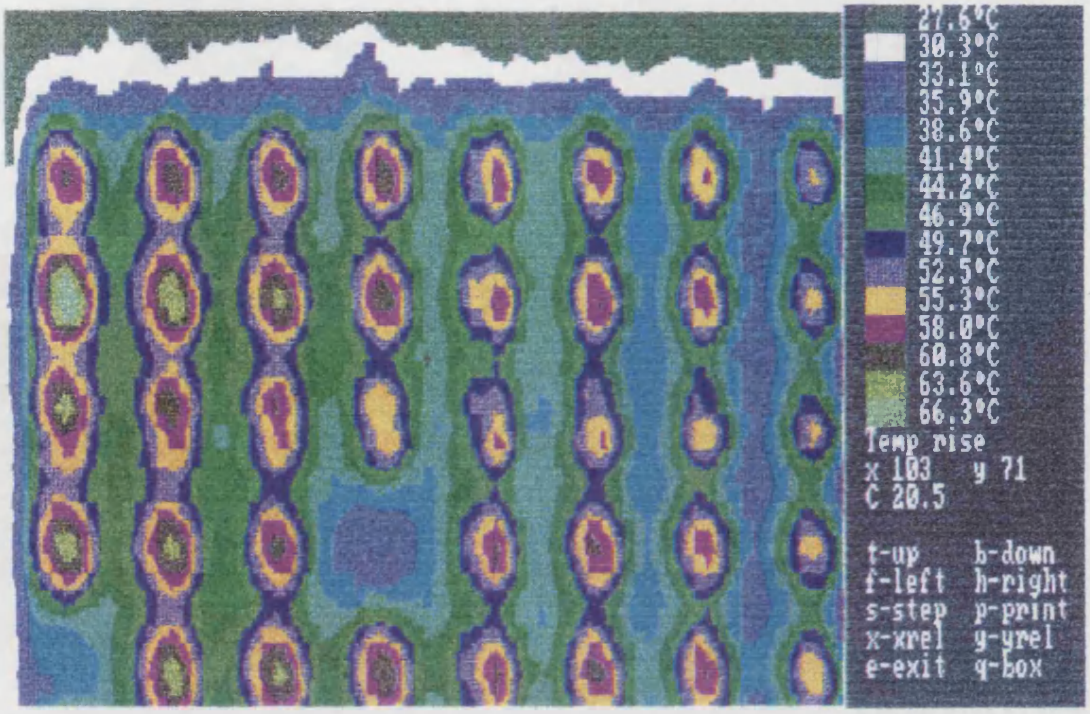


FIGURE 7.17a - THERMAL IMAGE OF SURFACE MOUNT TEST BOARD (POWER • 1 W/CHIP, V • 1.6 m/s)

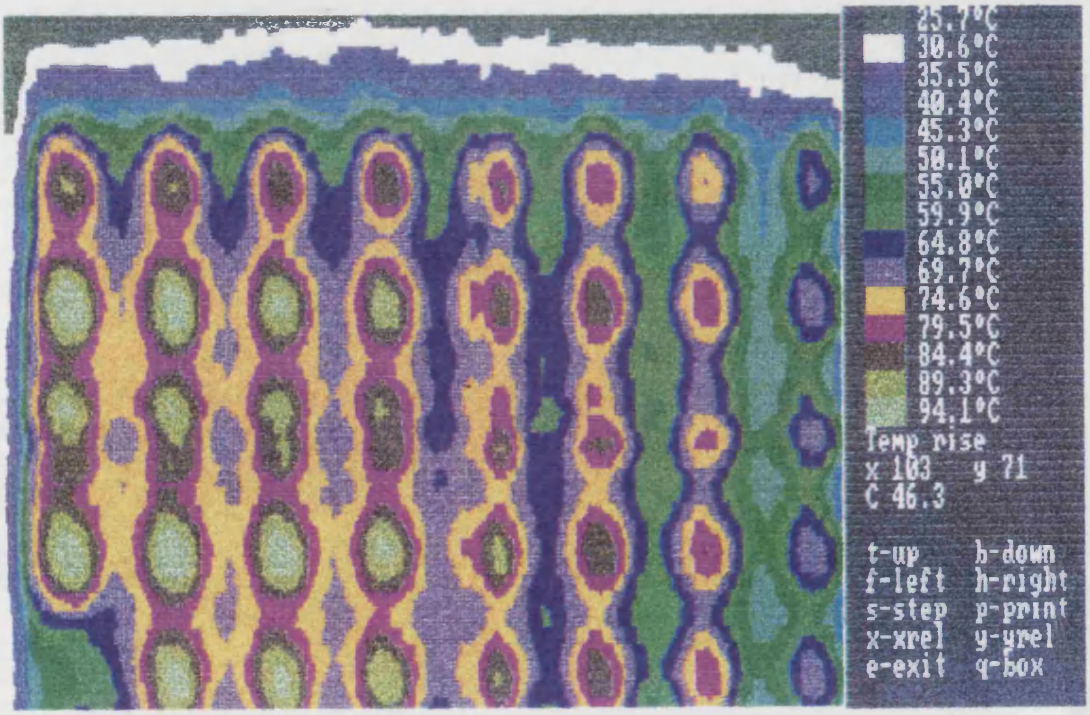


FIGURE 7.17b - THERMAL IMAGE OF SURFACE MOUNT TEST BOARD (POWER • 1.5 W/CHIP, V • 2.3 m/s)

FIGURE 7.18a
SURFACE TEMPERATURE OF PACKAGE ABOVE AIR INLET
TEMPERATURE FLOW VELOCITY 1.6 m/s

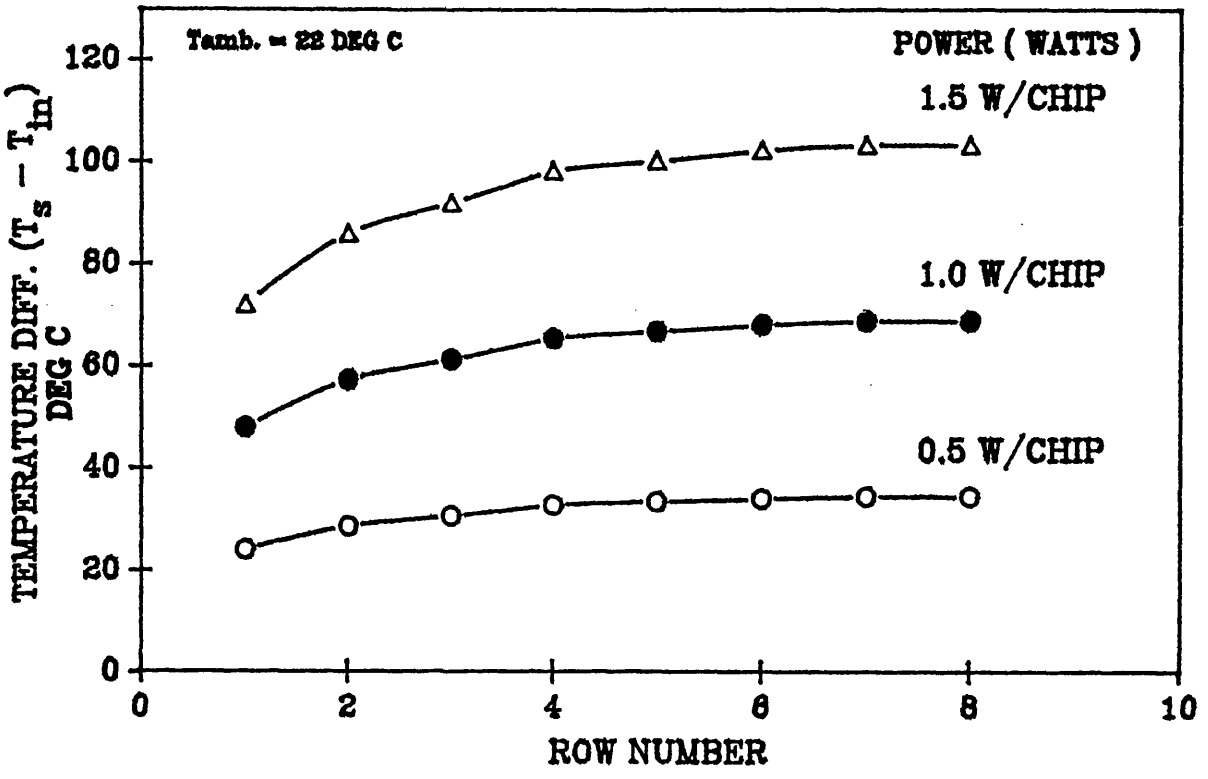


FIGURE 7.18b
SURFACE TEMPERATURE OF PACKAGE ABOVE AIR INLET
TEMPERATURE FLOW VELOCITY 2.3 m/s

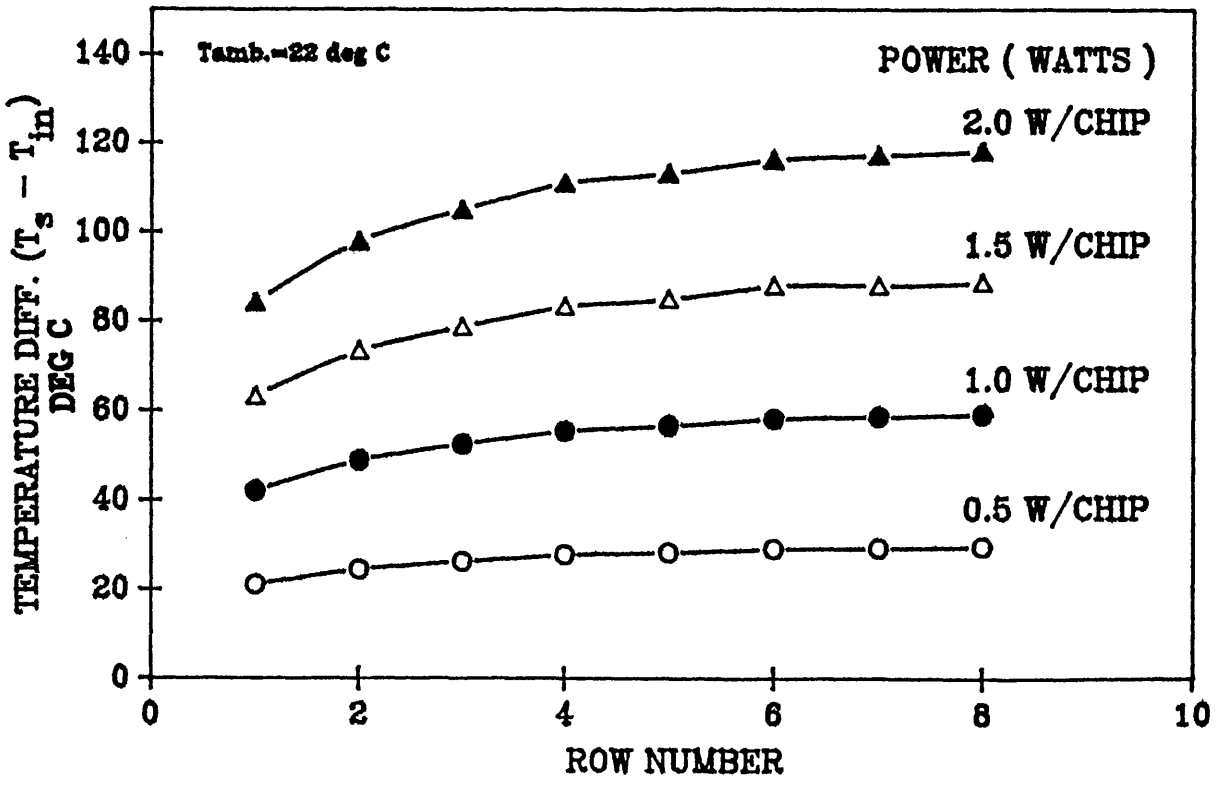


FIGURE 7.18c

SURFACE TEMPERATURE OF PACKAGE ABOVE AIR INLET TEMPERATURE FLOW VELOCITY 4.0 m/s

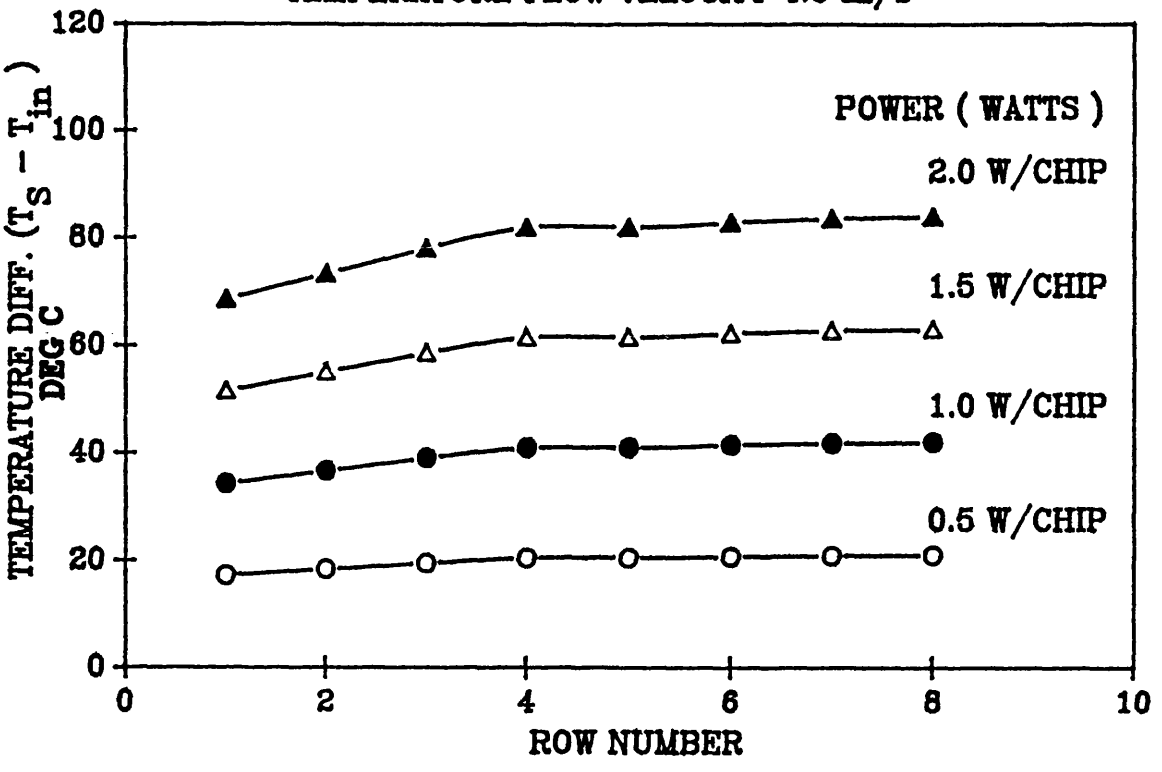


FIGURE 7.18d

SURFACE TEMPERATURE OF PACKAGE ABOVE AIR INLET TEMPERATURE FLOW VELOCITY 8 m/s

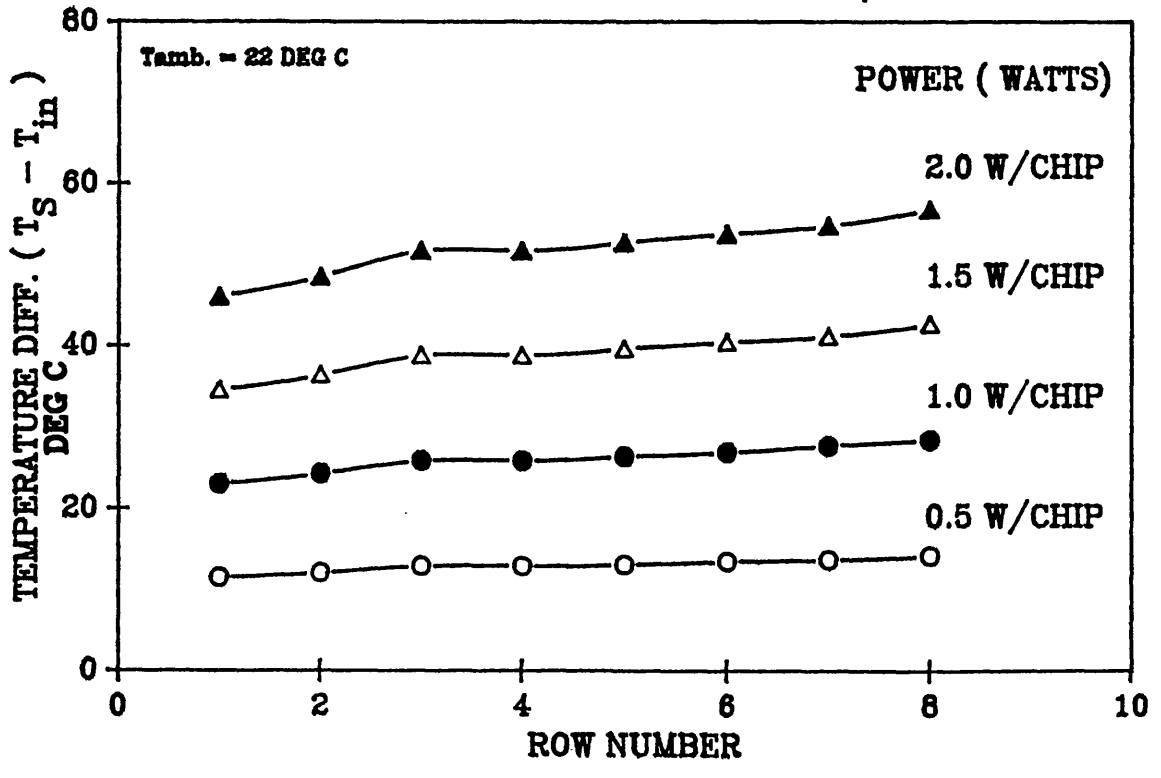


FIGURE 7.19

RELATION BETWEEN HEAT TRANSFER COEFFICIENT AND COMPONENT TEMPERATURE FOR FINITE ELEMENT MODEL

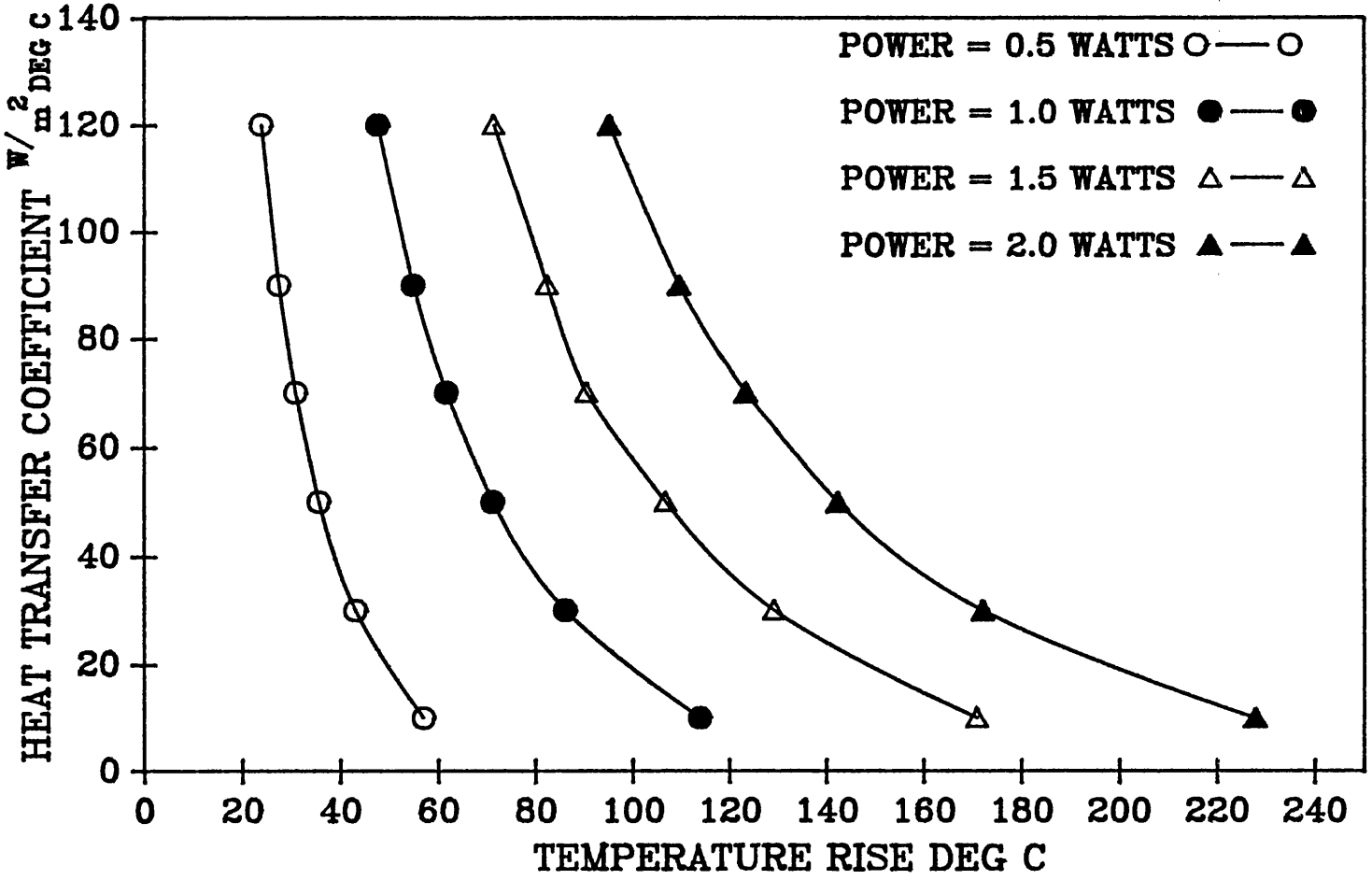


FIGURE 7.20

HEAT TRANSFER CORRELATION WITH REYNOLDS NUMBER INDEX 0.8

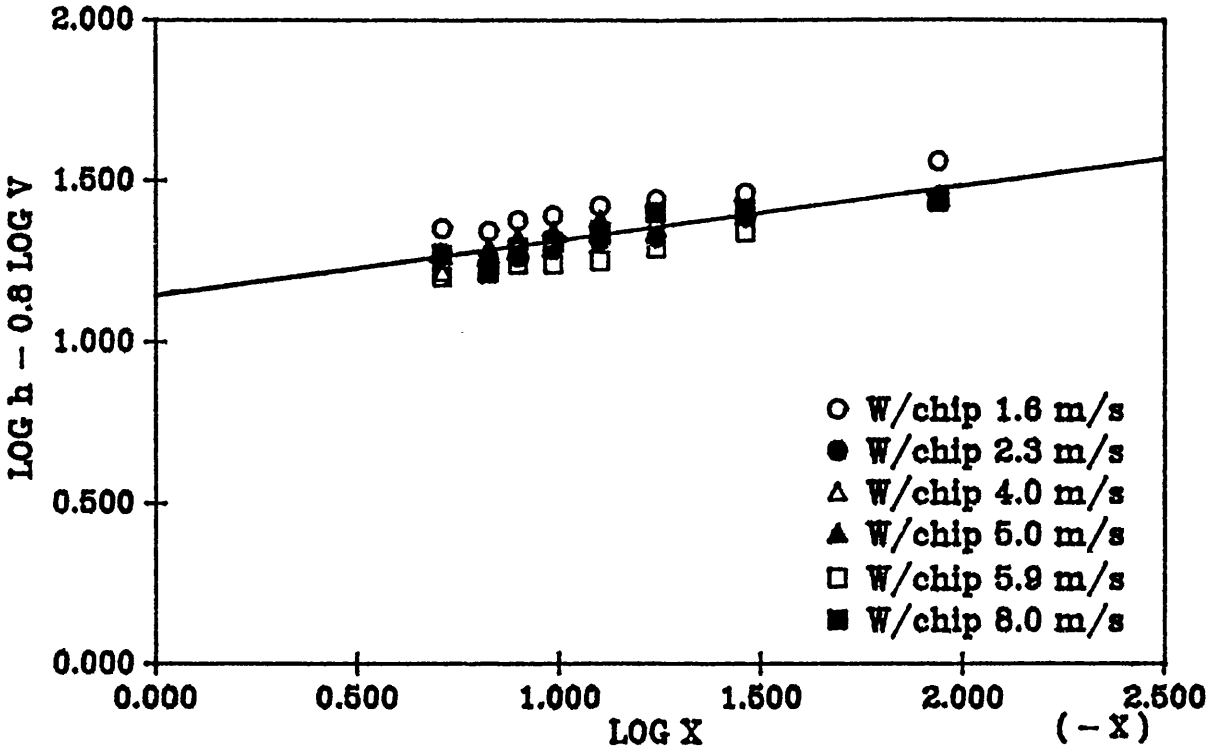


FIGURE 7.21

NUSSELT NUMBER AGAINST REYNOLDS NUMBER

CORRELATION FORM $Nu = C\ Re_x^{\ m}\ Pr^{1/3}$

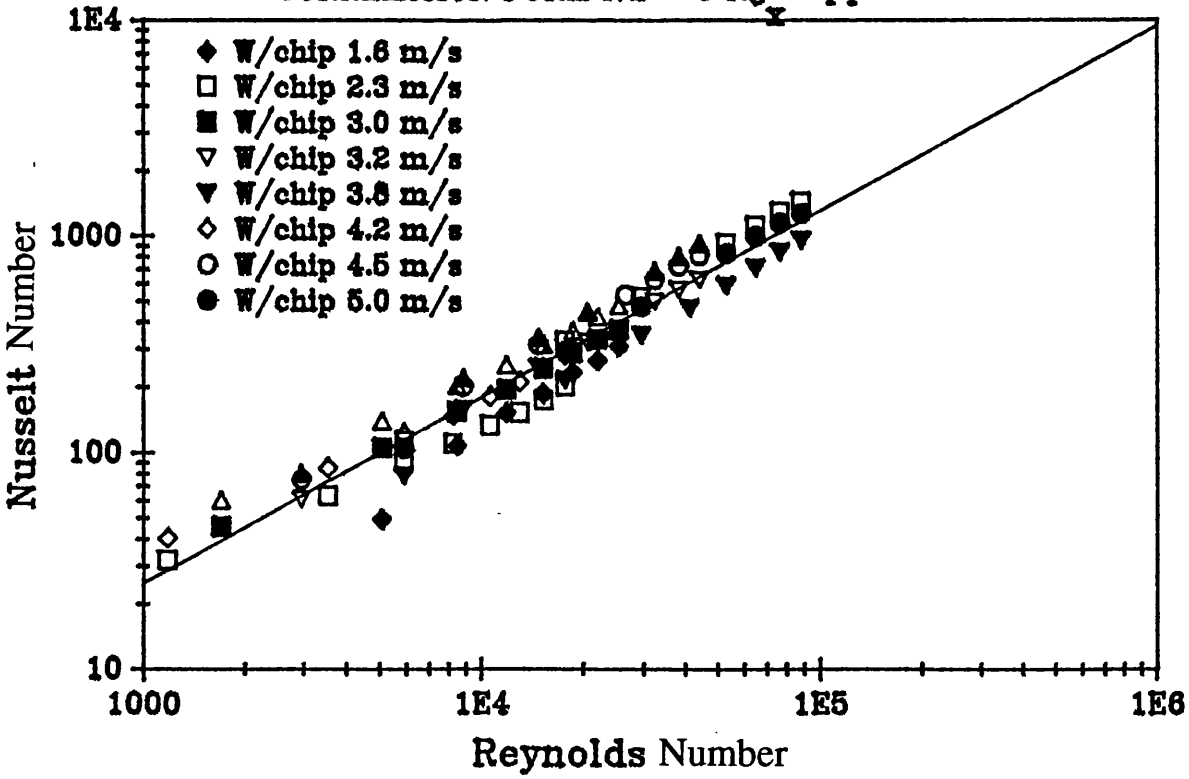


FIGURE 7.22a

COMPONENT TEMPERATURE DISTRIBUTION ALONG THE PCB

POWER DISSIPATION 0.5 W/CHIP

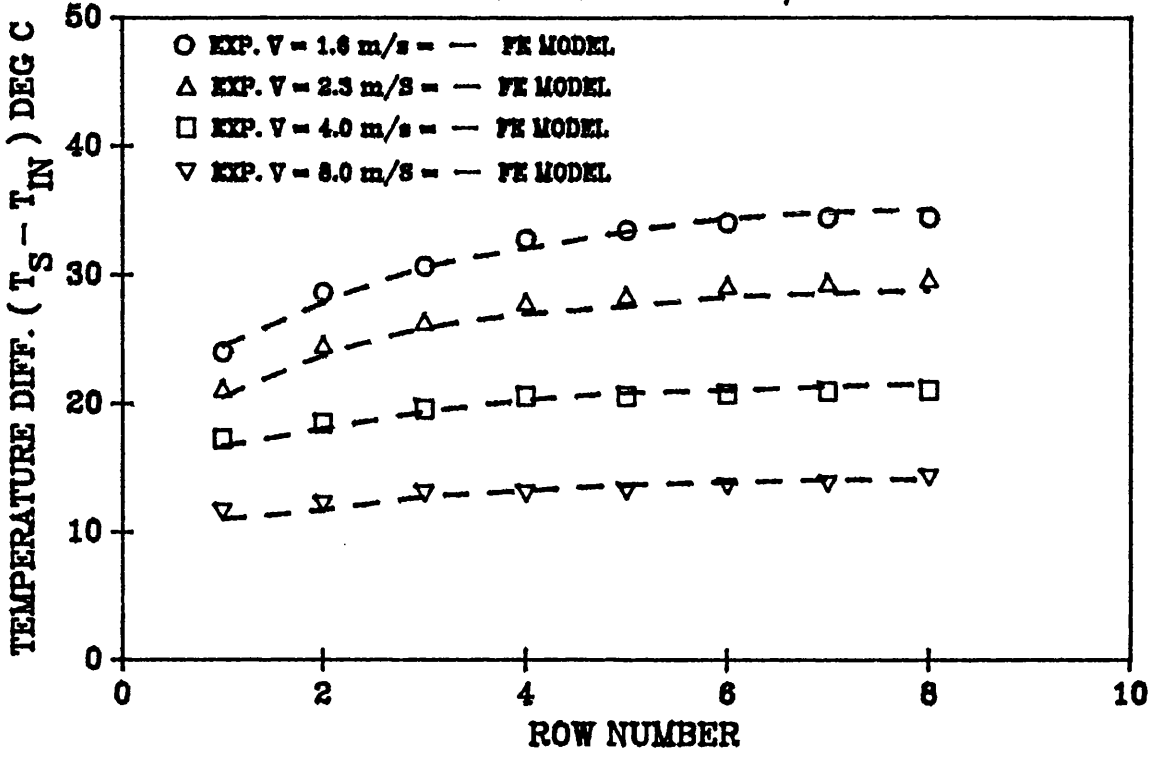
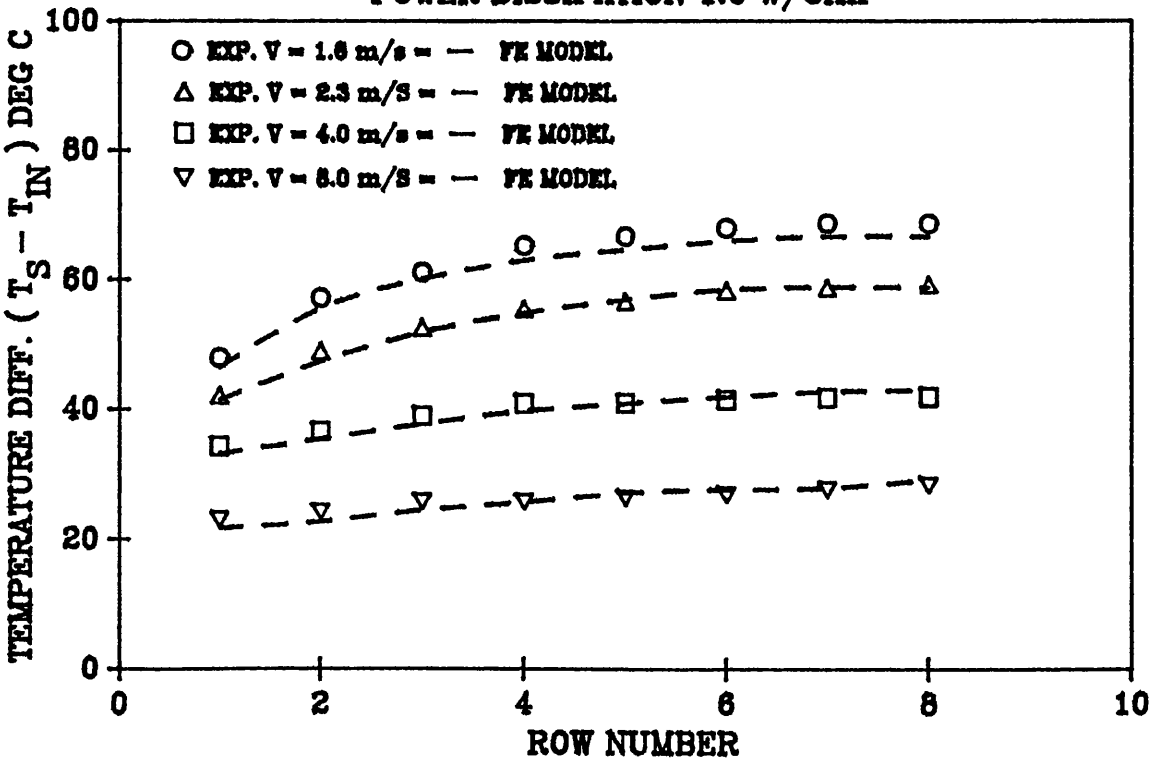


FIGURE 7.22b

COMPONENT TEMPERATURE DISTRIBUTION ALONG THE PCB

POWER DISSIPATION 1.0 W/CHIP



CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

8.1 GENERAL

The present work presents a detailed analysis of the complex three dimensional conduction/convection heat transfer process in miniature electronic modules mounted on a PCB. The objectives of this investigation were achieved by the design and development of experimental rigs, innovative instrumentation and detailed, realistic finite element models. For ease of understanding the conclusions in the following sections are arranged in such a way that, each section of the thesis is considered individually.

8.2 FINITE ELEMENT MODELLING OF ELECTRONIC PACKAGES

1 - In this investigation 3-dimensional finite element models of dual-in-line, chiprack and surface-mount packages were presented. In each case all constructional details of the package, which could affect its thermal performance, such as layout of leadframe, were accurately modelled.

2 - An important advantage of a FE model is the facility it provides to change individual design parameters systematically and in isolation. This facility was used to accumulate a great deal of steady-state and transient heat transfer data which are of direct interest to industry.

3 - The graphical output from the FE package has shown the complex three dimensional nature of the temperature distribution within the electronic packages modelled.

4- It is concluded that the FE method is better suited to handle detailed thermal analysis than the lumped parameter resistance network and finite difference method. The complex geometry of electronic packages was modelled without resorting to simplifying assumptions as in case of resistive networks.

8.3 REVIEW OF THE RESEARCH RIG AND EVALUATION OF HEAT TRANSFER COEFFICIENT

1 - The test rig was redesigned and modified. The forced draught system was changed to induced draught system thus giving undisturbed, well defined inlet conditions.

2- The temperature of each package on the test board was measured using a miniature bead thermistor glued at a convenient position under each package. This method of temperature measurement was found to be limiting, because it provided inadequate data to analyze the complex heat transfer process, and to validate the FE model.

3- The thermal and fluid boundary layers development in the test and dummy section was investigated. It was found that if the gap between the two boards does not exceed the package pitch the thermal and fluid boundary layers are successfully developed.

4 - Temperature distributions under different conditions of air speed and power dissipation were obtained. The heat transfer coefficient was evaluated at any streamwise location using two methods;

a) The test board was insulated with an identical board in back-to-back contact, both boards were powered to the same level. The total heat dissipation was convected to the airstream only from the top surface of the package and its associated board. The heat transfer coefficient was approximately evaluated using the rate equation.

b) A modified version of the finite element model presented by Hardisty et al [31] was used to match the experimental data by varying the heat transfer coefficient applied as boundary condition. The FE model also provided the detailed temperature distribution within the package and the board, from which the effect of the PCB on package temperature became evident.

5 - The investigation was extended to analyze the cooling of electronic packages under an array of impinging jets. The experimental results were correlated

using the FE model. Comparison was made with the published results of Colburn [56], Kern [57] and Huang [58]. The general trend of the h values from this investigation was found to be higher than the other investigators. this was thought to be the result of;

a) The manner in which the air was discharged from the rig, after passing through the jets.

b) The poor indication of the surface temperature of the package, because of badly positioned thermistor.

8.4 JUNCTION TEMPERATURE MEASUREMENT

1 - The feasibility of using a thin film thermocouple as a method of surface temperature measurement, based on the principle of sputtering process, was investigated. Although successful, the method was not favoured due to cost and time constraints.

2 - A brief description of the idealised concept of thermal resistance has been given. In addition, the advantages and disadvantages of various electrical techniques for measuring the junction temperature were described, and the preferred technique was discussed in detail. The technique selected for the present research, in which the forward-biased emitter-base junction of substrate isolation diode is used as a temperature sensitive parameter, can be used on all types of logic devices. The measurement procedure is relatively simple with a complex fast electronic switching circuit. This method is highly accurate because the temperature sensitive parameter is monitored under conditions that simulate normal device operation.

3 - Detailed circuit diagrams to enable the construction of complete test system for measuring the junction temperature using the V_{EB} have been presented. A calibration and extrapolation procedure to allow the method to be used in a production environment was described.

4 - The junction temperature measurement method was applied to a 14 pin duel-in-line package. Steady-state and transient thermal analyses of the DIP were presented. The thermal analysis is also complimented by a 3-dimensional finite element model. It was also shown that the FE model has made it possible to investigate the complex conduction path within a DIP. Good agreement between the theoretical and SID measurements was observed.

8.5 THERMAL INVESTIGATION OF CHIPRACK

1 - The thermal performance of a novel method of packaging (chiprack), designed and developed by Dowty Electronics, was investigated using the junction temperature measurement method. The 3-dimensional signal routing in the chiprack system has further complicated the three dimensional nature of heat transfer process in electronic systems.

2 - A comprehensive steady-state and transient study (in natural convection), complimented by a 3-dimensional FE model of the complete stack, revealed that the stack is being cooled largely by conduction to the mother board except at the uppermost level.

3 - The removal of the chip cover did not enhance natural convection cooling.

4 - Forced convection cooling of the complete stack mainly enhanced the cooling of the uppermost level and the mother board. To avoid damaging the un-encapsulated chip, forced convection cooling of the stack system without the chip cover was not carried out.

8.6 MECHANICAL INFRA-RED SCANNER

1 - The commercially available infra-red (IR) imaging system is very costly. This prompted the design and development of a custom built mechanical scanner using a static IR thermometer.

2 - An automatic data acquisition system controlled by a microcomputer was built.

3 - Comprehensive software was written to enable the user to set an automatic scanning routine and to convert the temperature array file into a meaningful thermal image.

4 - On completion, the scanner was incorporated into a forced convection cooling research rig.

5 - A comprehensive literature search of possible infra-red window materials was carried out. It was found that PROPAFILM "C" and cling film absorbs minimal radiation, on average 7% from 0 to 100°C. Cling film was used as the infra-red window in this investigation together with a correction factor

which was implemented in the temperature array file.

8.6.1 HEAT TRANSFER COEFFICIENT PREDICTION USING PRINCIPLE OF SUPERPOSITION OF THERMAL WAKE EFFECTS

1 - Detailed temperature distributions over a range of airspeed and power dissipations were obtained using the IR method.

2 - Heat transfer coefficients were obtained using the theory of the thermal wake, superposition (adiabatic temperature as reference fluid temperature) and a detailed FE model, under two conditions of uniform and non-uniform powering of the test board. It was shown that the adiabatic temperature rise of a passive module is influenced by the thermal wake it receives from the heated module upstream. The effect of a number of upstream heated modules (not necessarily at the uniform power) on the passive module will be the sum of the contribution of those heated modules upstream.

3 - In the fully developed region it was shown that the influence of heating one row, in isolation on the adjacent row, is the same as heating a row far down stream on its adjacent row. Furthermore the temperature rise of the powered rows in isolation remained the same.

4 - Theoretical data obtained from the FE model showed a satisfactory degree of agreement with the experimental data. Both experiment and theory demonstrated that the temperature rise of a module is the sum of the self-heating due to its internal heat generation and the wake it receives from upstream heating.

5 - The experimental heat transfer coefficient based on adiabatic temperature (h_{ad}) was compared with h_{bulk}, based on T_{bulk} (mixed mean temperature), presented by Hardisty and et al [31]. It was found that the heat transfer coefficient values were nearly the same over the first row only.

8.7 FORCED CONVECTION COOLING OF SURFACE MOUNT COMPONENTS

1 - The present work provides detailed heat transfer data on uniformly powered surface-mount packages (PLCC) mounted on a custom made printed circuit board (PCB).

2 - An experimental rig which simulates the PCB in a cabinet was constructed incorporating the mechanical IR scanner and SID pulsing board. An automatic data acquisition system was used to control the power dissipation in the test board.

3 - Thermal images providing the detailed temperature distribution under varying power dissipation and velocities were obtained. The investigation was also complimented with a realistic 3-dimensional theoretical FE model.

4 - Scarce values of thermal conductivity of plastic encapsulant were investigated and presented using two methods of;

a) combined FE and IR.
b) experiment.

Such thermal conductivity data are not available in the literature.

5 - Comparison of thermal resistance results obtained from the FE model (with deduced thermal conductivity) and those recommended by the manufacturers showed that the thermal resistance values obtained in this investigation was 3% higher than the recommended value. The effect of PCB on thermal resistance was also analyzed.

6 - The forced convection cooling of an array of surface mount components mounted on a printed circuit board was also investigated. The research reported here represents the first published correlation known to the author, with a particular emphasis on measurement and prediction of heat transfer coefficient.

8.8 RECOMMENDATION FOR FUTURE RESEARCH

The future FE research should be extended to include the problem of thermal stress. This is particularly important in the case of surface-mounted components, where the lack of flexibility in the leads increases the problems of fatigue, that arises from thermal mismatch.

Furthermore, since the combination of the thermal imaging and FE offers a powerful tool, it is recommended that the IR and FE data files are interfaced by a suitable software.

For the experimental investigations, consideration should be given to measurement of heat transfer coefficient using a heat flux meter. Unfortunately the miniature nature of the packages will make this a difficult task. However it may be possible to design and manufacture a custom made meter.

Detailed experimental analysis on a PCB should also address the conduction interaction of neighbouring packages. This could be undertaken by powering single module in isolation under reduced convection conditions.

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APPENDIX A1

PHYSICAL PROPERTY DATA BASE

A.1.1 THERMAL PROPERTIES OF MATERIALS COMMONLY USED IN ELECTRONICS PACKAGING

MATERIAL	THERMAL CONDUCTIVITY W/mK
ALUMINUM	205
ALUMINA	21
BERYLLIA	230
COPPER	398
DIAMOND	2300
GLASS EPOXY	1.7
GOLD	297
IRON	74.5
KOVAR (Fe, Ni, Co, Mn, C)	16.4
LEAD	34
MICA	0.50
MOLYBDENUM	138
NICKEL	92
PLATINUM	69
PORCELAIN	0.66
QUARTZ	1.01
RTV	0.31
SILICON	84
SILVER	418
SOLDER (95% Pb, 5% Sn)	36
THERMAL GLASS/PASTES	1.1
TIN	63

TABLE A.1.1 THERMAL CONDUCTIVITY OF PACKAGING MATERIALS AT 25°C

GAS	MEASURED AT °C	THERMAL CONDUCTIVITY W/mK
AIR	0	0.024
	100	0.030
ARGON	0	0.017
	63	0.019
HELIUM	7	0.144
	56	0.159
HYDROGEN	4	0.168
	50	0.186

TABLE A.1.2 THERMAL CONDUCTIVITY OF SELECTED GASES AT ONE ATMOSPHERE

LIQUID	THERMAL CONDUCTIVITY W/mK
WATER	0.60
FREON 113	0.073
FC-72	0.058
FC-75	0.065
FC-77	0.0065
MINERAL OIL	ABOUT 0.15

TABLE A.1.3 THERMAL CONDUCTIVITY OF SELECTED LIQUIDS AT 25 °C

INSULATOR	DIELECTRIC CONSTANT	THERMAL EXPANSION COEFFICIENT 10^{-7} / °C	THERMAL CONDUCTIVITY W/mK
NON-ORGANIC:			
92% ALUMINA	9.2	60	18
96% ALUMINA	9.4	66	20
SI_3N_4	7	23	30
SiC	42	37	270
AlN	8.8	33	230
BeO	6.8	68	240
BN	6.5	37	600
DIAMOND			
HIGH PRESSURE	5.7	23	2000
PLASMA CVD	3.5	23	400
GLASS-CERAMICS	4-8	30-50	5.0
COPPER CLAD INVAR (10% COPPER)/ (GLASS COATED)	-	30	100
GLASS COATED STEEL	6	100	50
ORGANIC:			
EPOXY-KEVLAR(X-Y) (60%)	3.6	60	0.2
POLYIMIDE-QUARTZ (X-AXIS)	4.0	118	0.35
Fr-4(X-Y PLANE)	4.7	158	0.2
POLYIMIDE	3.5	500	0.2
BENZOCYCLOBUTENE	2.6	350-600	0.2
TEFLON	2.2	200	0.1

TABLE A.1.4 PROPERTIES OF PACKAGE INSULATOR MATERIAL

METAL	MELTING POINT °C	ELECTRICAL RESISTIVITY 10^{-6} OHM cm	THERMAL EXPANSION COEFFICIENT 10^{-7}/°C	THERMAL CONDUCTIVITY W/mK
COPPER	1083	1.7	170	393
SILVER	960	1.6	197	418
GOLD	1063	2.2	142	297
TUNGSTEN	3415	5.5	45	200
MOLYBDENUM	2gw5	5.2	50	146
PLATINUM	1774	10.6	90	71
PALLADIUM	1552	10.8	110	70
NICKEL	1455	6.8	133	92
CHROMIUM	1900	20	63	66
INVAR	1500	46	15	11
KOVAR	1450	50	53	17
SILVER-PALLADIUM	1145	20	140	150
GOLD-PLATINUM	1350	30	100	130
ALUMINUM	660	4.3	230	240
Au-20% Sn	280	16	159	57
Pb-5% Sn	310	19	290	63
Cu-W(20%Cu)	1083	2.5	70	248
Cu-Mo(20%Cu)	1083	2.4	72	197

TABLE A.1.5 PROPERTIES OF PACKAGE CONDUCTOR MATERIAL

SUBSTRATE/PROPERTY	Tg	CTE	K	E	ε
EPOXY FIBREGLASS	125	140-180	0.16	35	4.8
POLYIMIDE FIBREGLASS	250	120-160	0.35	40	4.8
EPOXY ARAMID FIBRE	125	60-80	0.12	60	3.9
POLYIMIDE ARAMID FIBRE	250	50-80	-	4.0	56
EPOXY QUARTZ (FUSED SILICA)	125	60-120	-	-	-
POLYIMIDE QUARTZ (FUSED SILICA)	250	60-120	-	-	-
FIBREGLASS/ARAMID (FIBRE COMPOSITE)	125/250	50-80	-	-	-
FIBREGLASS/TEFLON LAMINATES	75	200	0.26	3	2.3
ALUMINA-BERYLLIA CERAMIC	NA	50-70	21.0	560	8.0

KEYS:
Tg = GLASS TRANSITION TEMPERATURE (DEG C)
CTE = COEFFICIENT OF THERMAL EXPANSION (10-7/DEG C) K = THERMAL CONDUCTIVITY (W/mK)
E = IN PLANE TENSILE MODULUS (GPa) ε = DIELECTRIC CONSTANT AT 1 MH

TABLE A.1.6 GENERAL SUBSTRATE MATERIALS

SUPPLIER	COMPOUND NO.	THERMAL CONDUCTIVITY W/mK	THERMAL EXPANSION $10^{-7}/°$	FLEXURAL STRENGTH GPa	FLEXURAL MODULUS GPa
SUMITOMO	EME-1100-T	0.67	200	0.14	15.66
	EME-1100-H	0.67	200	0.14	15.66
	EME-1100-K	0.67	200	0.14	14.19
	EME-6200	0.67	200	0.13	12.72
	EME-6300	0.42	170	0.13	12.23
	EME-9100-XK	0.67	200	0.14	14.19
	EME-9200	0.67	200	0.13	12.72
	EME-9300	0.42	170	0.13	12.23
	EME-5000LS	0.67	200	0.15	14.68
PLASKON	3100	1.0	270-750	0.14	14.68
	3100LS	0.71	210-600	0.14	14.68
	3200	1.0	270-750	0.15	14.68
	3200LS	0.71	220-600	0.15	14.68
	3300	1.0	270-750	0.15	14.68
	3300LS	0.71	210-600	0.15	15.81
	3300SH	0.71	210-600	0.157	15.81
HYSOL	MG15f	0.71	250-700	0.12	13.76
	MG35F	1.46	260-750	0.13	14.44
	MG36f	0.75	170-700	0.13	13.76
NITTO	HC10-2	0.63	200-700	0.15	13.70
	HC20-2	0.92	240-700	0.15	13.70
	HC30-2	1.46	260-700	0.15	14.68
	HC50-2	1.97	250-700	0.15	14.68
	MP119	0.63	180-650	0.13	12.23
	MPX-75	0.71	200-650	0.16	14.19
	MP150	0.71	160-740	0.13	11.74
	MP150-164	0.71	160-740	0.13	11.74

TABLE A.1.7 PROPERTIES OF SEMICONDUCTOR MOLDING COMPONENT

APPENDIX A2

CALCULATION OF POWER DISSIPATION IN THE TEST CHIP

A.2.1 METHOD OF POWER CALCULATION

The power being applied to the test chips is dependent on the Mark Space Ratio (MS) of the input signal to the logic gates. For example, a 10% S ratio, the logic gates are on for 10% of the cycle time and off for 90% of the time.

The following formula is used in the calculation of power:-

$$P_{chip} * I_{chip}$$

Figure A1 shows the set up of the test chip therefore:-

$$V_{chip} = V_h - V_L$$

$$I_{CHIP} = \frac{(V_h - V_{RD})}{R_{CC}} \qquad \text{(A1)}$$

R_{cc} is known, but V_h, V_L, V_H and V_{RD} must be measured twice, once when the logic is state 1 (on) and once when the logic state is 0 (off). This yields two powers P_{on} and P_{off}, then the following is used to calculate the overall power to the chip.

$$TOTAL\ POWER = P_{on}t_{on}\% + P_{off}t_{OFF}\% \qquad \text{(A2)}$$

Where $t_{on}\%$ and $t_{off}\%$ are the percentage time the chips logic gates are on and off

respectively.

A.2.2 CALCULATION OF POWER FOR TEST CARRIED OUT

The required voltages were measured at on-time and off-time. The above method was then used to calculate the power input to the chips.

Measured values:-

ON TIME	OFF TIME
V_h = 4.8 V V_H = 6.5 V_{RD} = 5.8 V_L = 1.04	V_h = 5.6 V V_H = 6.6 V_{RD} = 6.4 V_L = 0.092

With R_{cc} = 10.0 Ω, this yielded:-

MARK SPACE RATIO	POWER (W)
10%	0.13
20%	0.14
30%	0.16
40%	0.17
50%	0.19

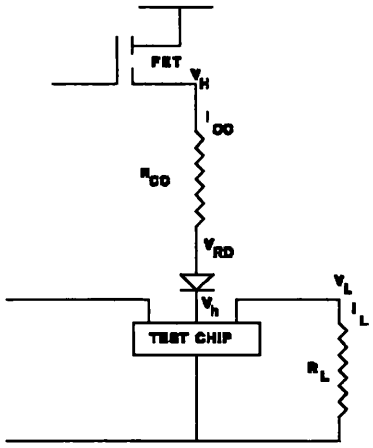


FIGURE A2.1-THE CIRCUIT FOR CALCULATION OF POWER DISSIPATION

APPENDIX A.3

POTENTIAL INFRA-RED WINDOW MATERIALS

A.3.1 TEST FOR INFRA-RED TRANSMISSIVITY

A potential material to be used as infra-red window in forced convection research rig must have the following characteristics:-

a) Absorb the minimum amount of radiation

b) Permit air tight seal in test section

c) preserve the experiment repeatability

d) Not to be prohibitive on cost ground

After a comprehensive literature search three materials were selected. The chosen materials are very low in cost and a comparison of their radiation absorbtion was made.

i) perspex

ii) "Propafilm" C

iii) Cling film

Although it was revealed that such material as Germanium, Quartz and Natural type 2A Diamond have excellent transmissive characteristics, they were not considered on cost ground.

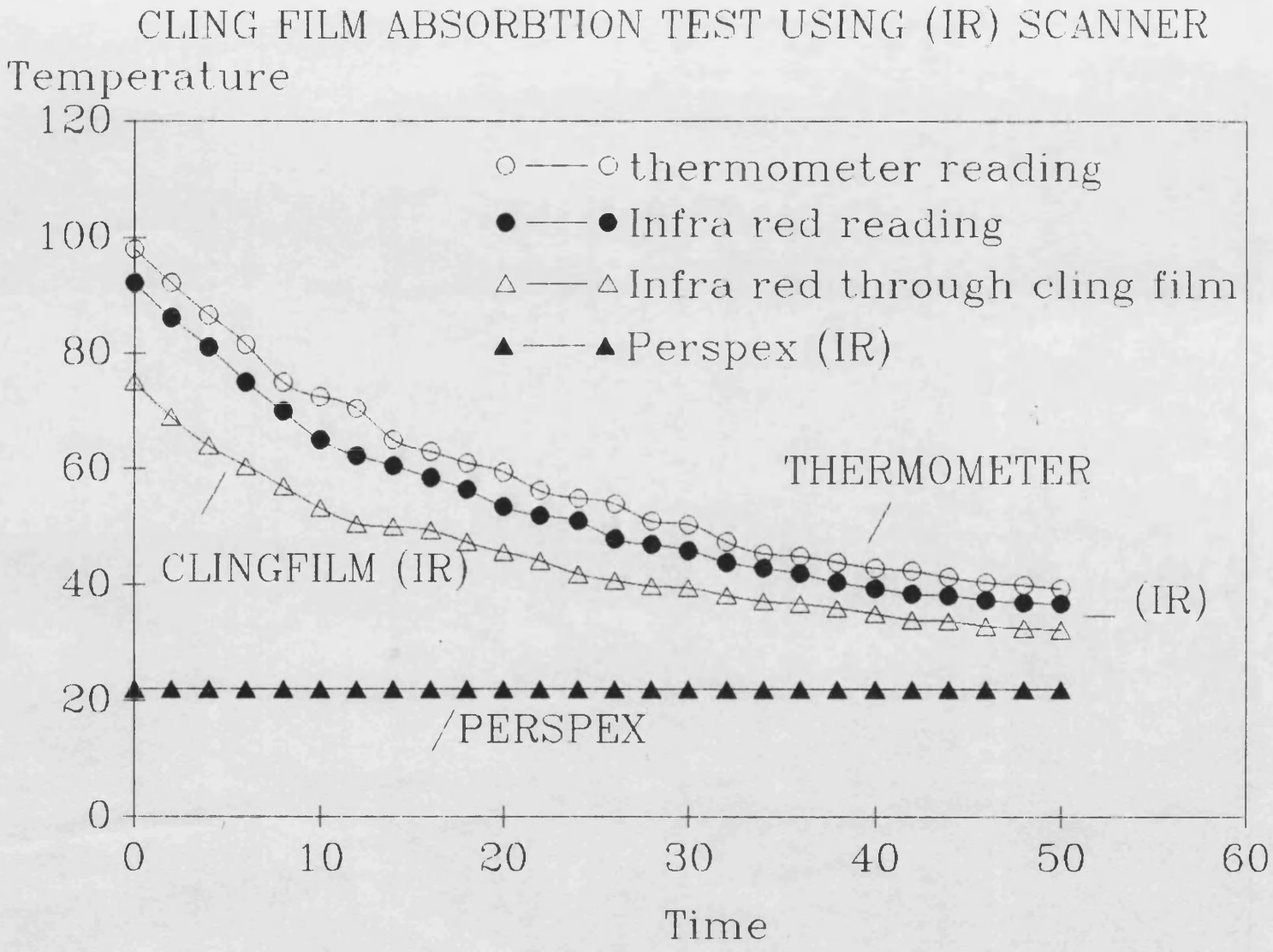
A.3.2 METHOD OF TESTING

A bomb calorimeter was filled with water and heated with a bunsen burner to boiling point. The water was well stirred and its temperature was measured by a thermometer clamped in a stand. The outside copper body of the calorimeter was painted mat black ($\varepsilon \simeq 1$) and its temperature was monitored without any interfering medium, after the heater had been switched off, with the infra-red thermometer described in Chapter 6. Total of three experiments was then performed with a sheet of above mentioned material stretched over a purposely built frame, which was placed between the infra-red instrument and the calorimeter. Figure A.3.1 illustrates the cooling curve obtained for the three materials tested. As shown, the cling film window caused a maximum temperature reduction from the infra-red detector of 17°C, when the thermometer reading was 98.5°C. This temperature disparity progressively reduced towards zero as the calorimeter temperature approached ambient.

A.3.3 CONCLUSION

The results show, depending up on the operating temperature of the measuring surface, a significant but predictable degree of absorbtion of infra-red by cling film and Propafilm C. Since the materials gave the same test results, and are both freely available, their mechanical properties governed their use as potential window material. The stretching of the cling film was particularly attractive because it could be stretched under tension on the perspex frame (duct window for infra-red). The problem of cling film absorbtion was overcome by a correction factor to every read temperature during the test if the window was employed. The correction factor was

implemented in the image processing program by storing the true values of temperature in an array : TEMP (IR-TEMP) and mapping the infra-red detected temperature values to the true temperatures for every temperature read during the test. In the case of natural convection tests where no interfering medium exists a facility was provided in the program to over ride the compensation option.


CLING FILM ABSORBTION TEST USING (IR) SCANNER
Temperature
120
100
80
60
40
20
0
thermometer reading
Infra red reading
Infra red through cling film
Perspex (IR)
THERMOMETER
CLINGFILM (IR)
(IR)
/PERSPEX
0
10
20
30
40
50
60
Time